Product Brochure

Anritsu

MP1800A Series

Signal Quality Analyzer

Compact and High-performance BERT
32.1 Gbit/s Signal Quality Analyzer

MP1800A SQA is a modular BERT with plug-in modules;

- Pulse Pattern Generator (PPG) supporting high quality output and high amplitude signals
- Error Detector (ED) with high input sensitivity supporting signal analysis, such as Bathtub and Eye Diagram measurements
- Jitter Modulation Source (JMS) for generating various types of jitter, such as SJ/RJ/BUJ/SSC, and supporting Jitter Tolerance tests

MP1800A supports physical layers testing for optical modules and highspeed devices up to 32.1 Gbit/s. Combined use with the MP1821A 50G/56G bit/s MUX and MP1822A 50G/56G bit/s DEMUX supports BER tests up to 56 Gbit/s. Moreover, powerful signal integrity tests at up to 28.1 Gbit/s are supported by linked operation with the MP1825B 4Tap Emphasis.

Wide Bandwidth 0.1 Gbit/s to 32.1 Gbit/s

32.1 Gbit/s Jitter Tolerance Test (SJ, RJ, BUJ, SSC)

Signal Quality Analysis

Optical Interfaces

High-quality, Low-jitter Waveforms

High Input Sensitivity & Wide Phase Margin

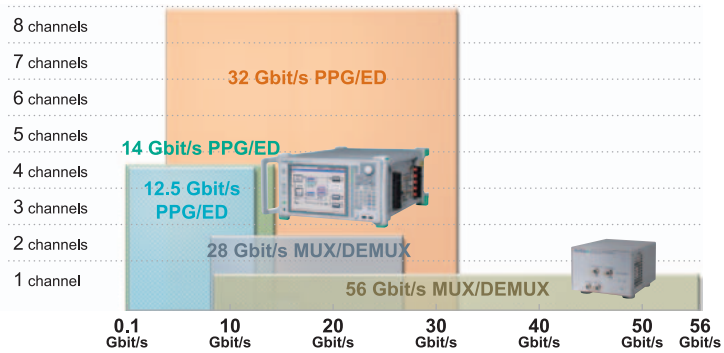
Burst Measurement

Multi-channel Configuration (Up to 8ch)

Wide Bandwidth 0.1 Gbit/s to 32.1 Gbit/s

Supports 0.1 Gbit/s to 32.1 Gbit/s bit rate thru module selection

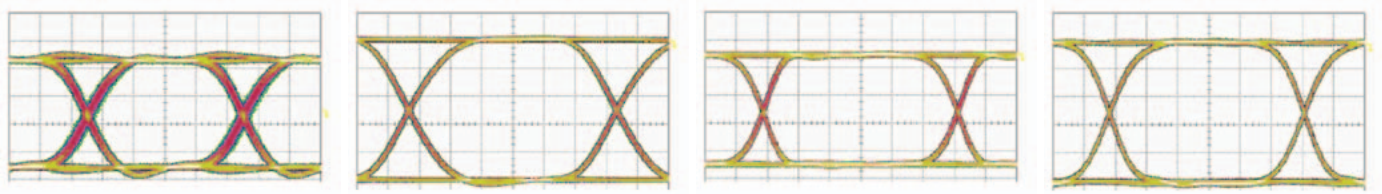
- 2.4 Gbit/s to 32.1 Gbit/s:
  MU183020A/21A, MU183040A/41A (Option-001)
- 2.4 Gbit/s to 28.1 Gbit/s:
  MU183020A/21A, MU183040A/41A
- 8 Gbit/s to 28.1 Gbit/s:
  MU182020A/21A, MU182040A/41A (Option-001/003)
- 8 Gbit/s to 28 Gbit/s:
  MU182020A/21A, MU182040A/41A (Option-001)
- 8 Gbit/s to 25 Gbit/s:
  MU182020A/21A, MU182040A/41A
- 0.1 Gbit/s to 14 Gbit/s:
  MU181020B, MU181040B (Option-002)
- 0.1 Gbit/s to 14.05 Gbit/s:
  MU181020B, MU181040B (Option-002/003)
- 0.1 Gbit/s to 12.5 Gbit/s:
  MU181020A, MU181040A (Option-002)
- 9.8 Gbit/s to 12.5 Gbit/s:
  MU181020A, MU181040A (Option-001)



Low-jitter High-quality Waveforms

The combination of low-jitter, high-quality output waveform, and high-amplitude output PPG and MUX modules can be tailored to the application.

- Low Jitter: 8 ps p-p (MU181020A/B-012)
- High Amplitude: 0.5 Vp-p to 3.5 Vp-p (MU181020A/B-013, MU182020A/21A-013)

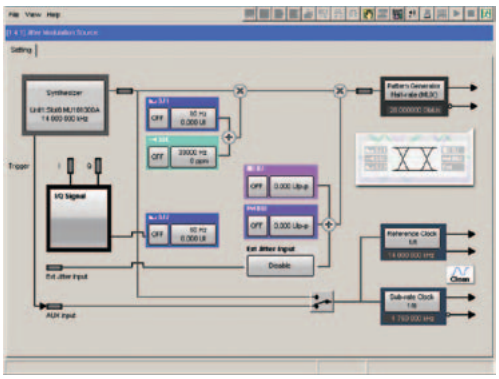


MU181020A-010 **MU181020A-011** **MU181020A-012** **MU181020A-013**

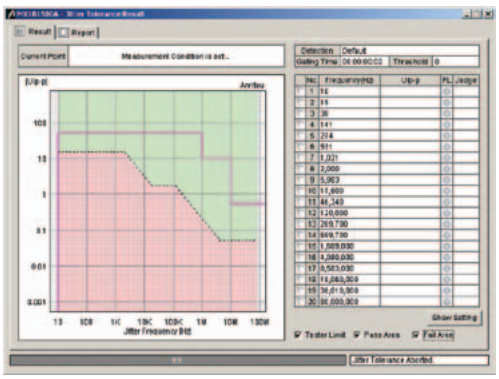
10 Gbit/s, PRBS31, Maximum amplitude

SJ, RJ, BUJ and SSC Modulation Source Supporting Interconnect Standards up to 32.1 Gbit/s

The intrinsic jitter of the clock output from the MU181500B Jitter Modulation Source is less than 350 fs rms, supporting low-jitter clocks. The combination of low-jitter waveform with excellent jitter transparency supports high-accuracy jitter tolerance tests. Moreover, simultaneous injection of RJ, BUJ and SSC as well as two SJ for two-tone support required by PCIe enables a variety of jitter tolerance tests. In addition, the MX181500A Jitter/Noise Tolerance Test Softwave supports multi-mask tables as standard as well as easy mask editing to support future next-generation standards.

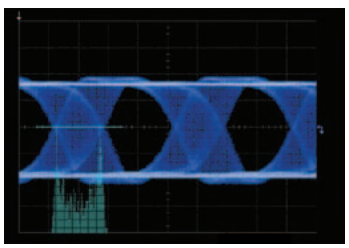


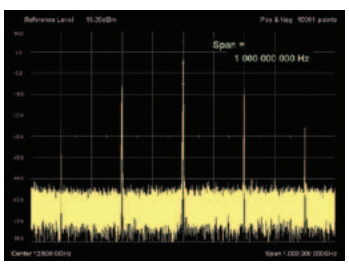
MU181500B Jitter Modulation Source setting screen



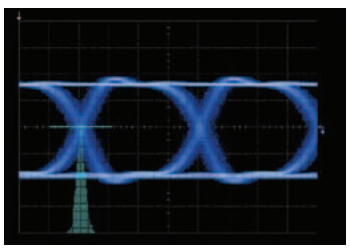
MX181500A Jitter/Noise Tolerance Test Software setting screen

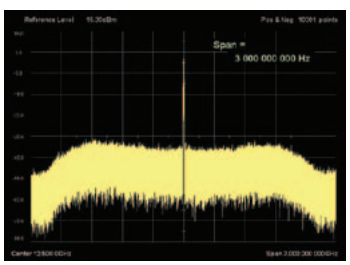
Sine-wave jitter (SJ)



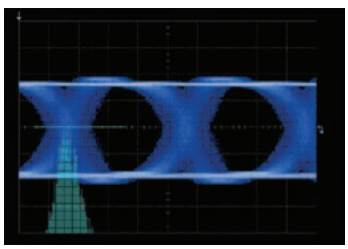


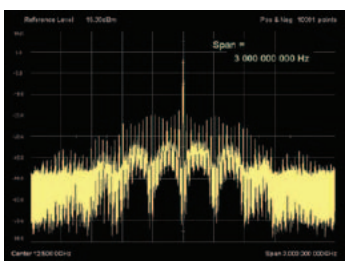
Random jitter (RJ)





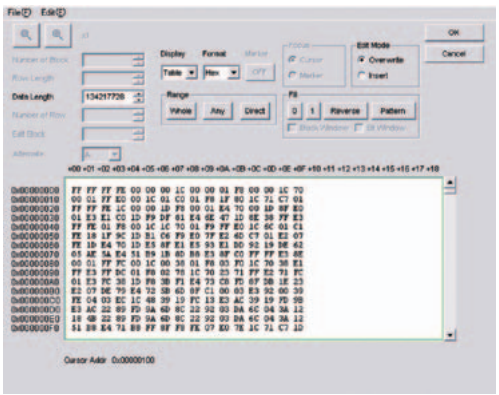
Bounded uncorrelated jitter (BUJ)





Versatile Pattern Generation

- Pseudorandom patterns (PRBS)
  Because all PRBS rates required by the standards are supported up to PRBS2^{31}–1, all BER are supported.
  2^n–1 (n = 7, 9, 10, 11, 15, 20, 23, 31)
- Zero Substitution Pattern
  All 0s and All 1s patterns can be added to PRBS patterns for performing CDR tolerance tests.
  2^n, 2^n–1 (n = 7, 9, 10, 11, 15, 20, 23)
- Data Pattern
  Patterns required by each application can be created with flexibility.
  128 Mbits max. (Steps: 1-bit)
- Alternate Pattern
  Two patterns (A and B) can be set and the A/B pattern can be output at any timing.
- Mixed Pattern
  A mixed data and PRBS pattern can be output. At creation of SONET/SDH frames, adding a PRBS2^{31}–1, etc., pattern to the payload allows setting of a continuous pattern across frames.
- Sequence Pattern
  A variety of programmable patterns can be output in any sequence and combining various patterns offers effective support for applications requiring sequence processing.



Data Pattern Setting Screen

High Input Sensitivity & Wide Phase Margin

Using the high-input sensitivity ED Rx function supports direct input and evaluation of low-amplitude data.

- Input Sensitivity
  MU181040A-001: <50 mVp-p
  MU181040A/B-002: 10 mVp-p (typ.)
- Phase Margin
  MU181040A/B-002: 60 ps (typ.) (12.5 Gbit/s)

Burst Measurement

The following application evaluations using burst signals are supported.

- E-PON, G-PON, 10GE-PON Upstream Test
- Optical Loop Test
- Transmission Test using Quantum Noise Technology

Optical Interface

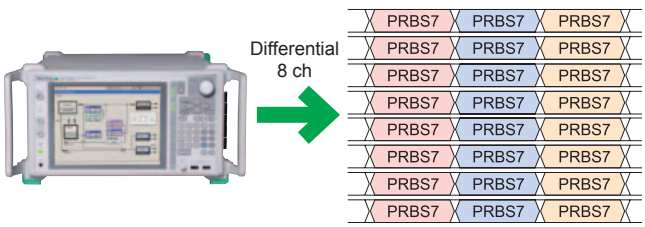
Supports Two Optical Interface Types

- MU181600A/01A
  Supported wavelengths and bit rates for SFP and XFP modules can be customized freely by changing modules.
- MU181620A/40A
  These options are used for the 10GbE stressed eye test; the output power and extinction ratio can be changed as necessary using the 0.1 to 12.5 Gbit/s wideband E/O, O/E converter.

Multi-channel Configuration

Due to the modular platform design, the PPG/ED modules can be configured with various other modules to build a custom system. Additionally, crosstalk and skew tolerance are easily evaluated by synchronizing several PPG patterns and shifting phases.

∗: For details about possible module combinations, see the Option Selection Guide for the MP1800A series.

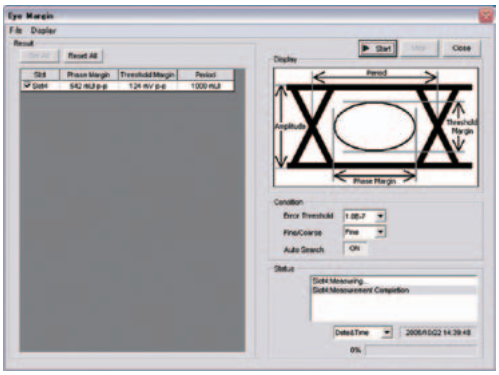


MP1800A Pattern Timing when Sending PRBS7 on All Channels (Pattern Sync)

∗: Functions and specifications are different according to the module. Refer to the Specification and Brochure for each module.

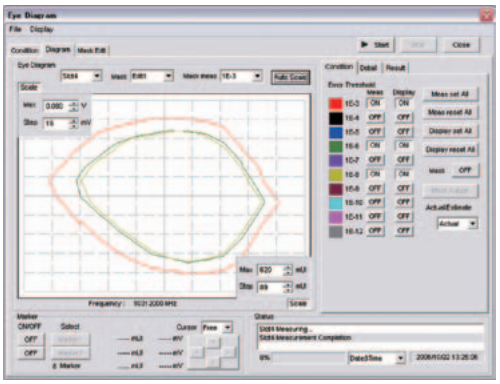
Eye Margin

For confirming DATA threshold and phase margins.



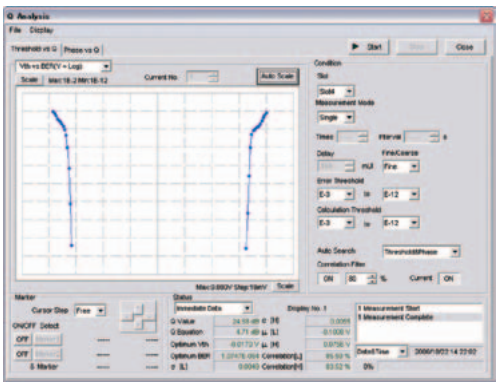
Eye Diagram

Used to obtain bit error rate contours linking specified bit error rate points.



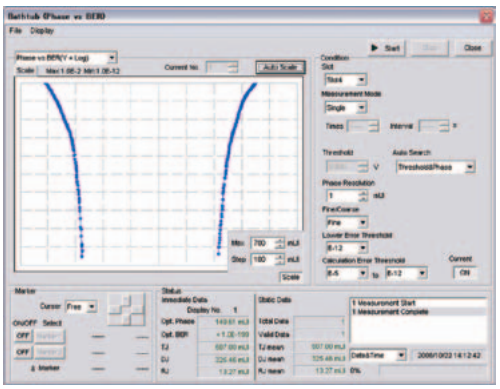
Q Measurement

Calculates Q value from bit error rate using change in threshold value. Can be used to check change in Q value for clock phase.



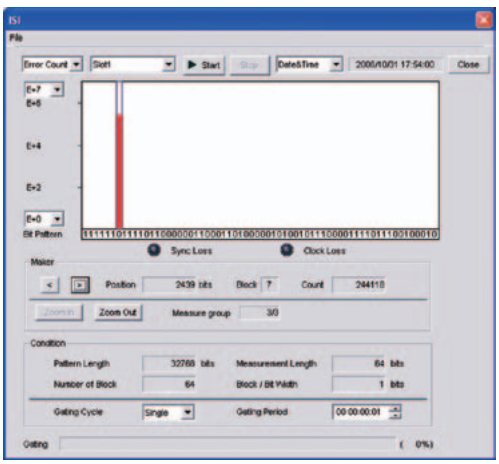
Bathtub

Performs optimum bit error rate based on changes in bit error rate relative to phase. And performs jitter analysis (TJ, DJ, RJ).



Bit Error Analysis using ISI

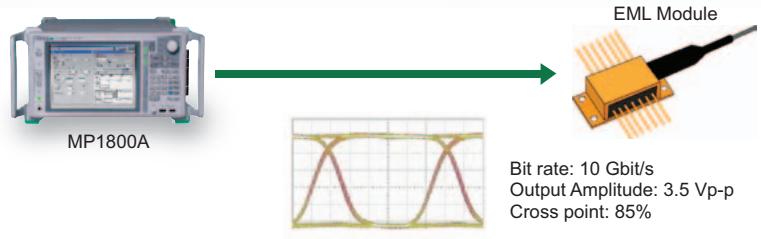
Used to confirm bit error rate in each specified block or bit position and for bit error rate correlation with inter-symbol interference.



∗: Functions and specifications are different according to the module.
Refer to the Specification and Brochure for each module.

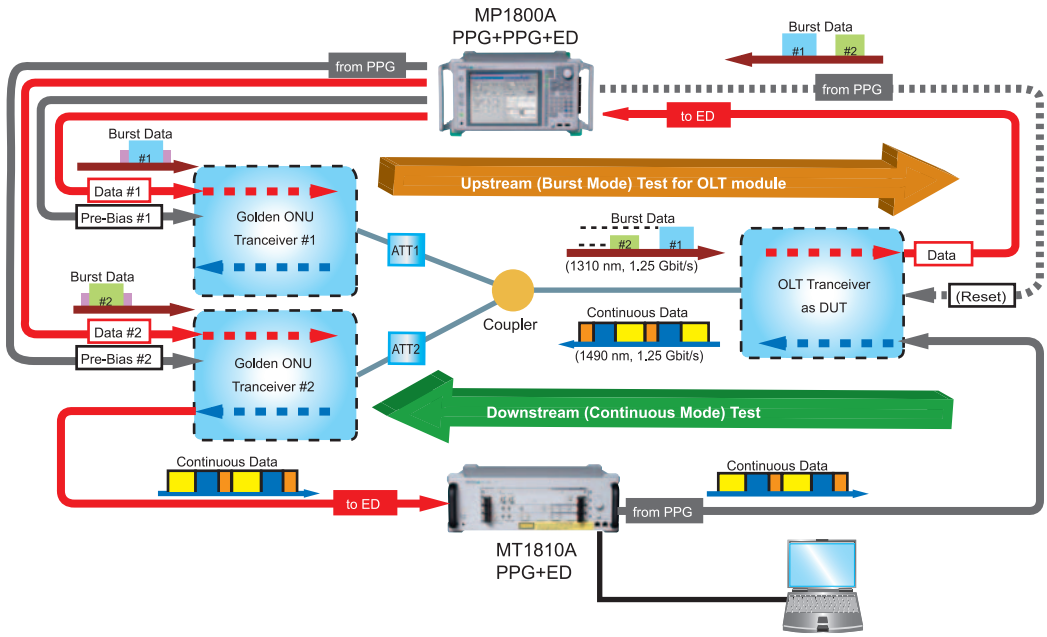
Applications

Application 1: EA/EML Module Evaluation



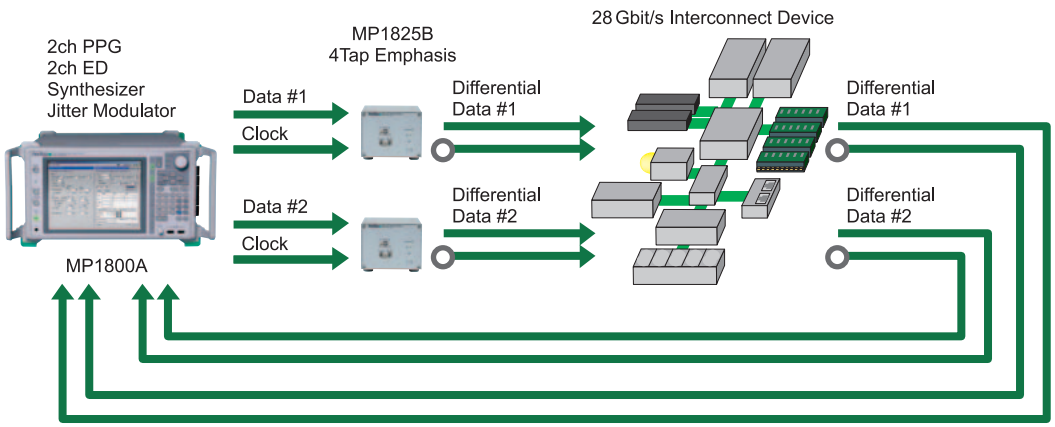
- Direct driving of EML and EA module using 3.5 Vp-p high-amplitude waveform
- Wide cross point adjustment function: 20 to 90% [MU181020A/B-013]

Application 2: 10 Gbit/s PON OLT Module Inspection



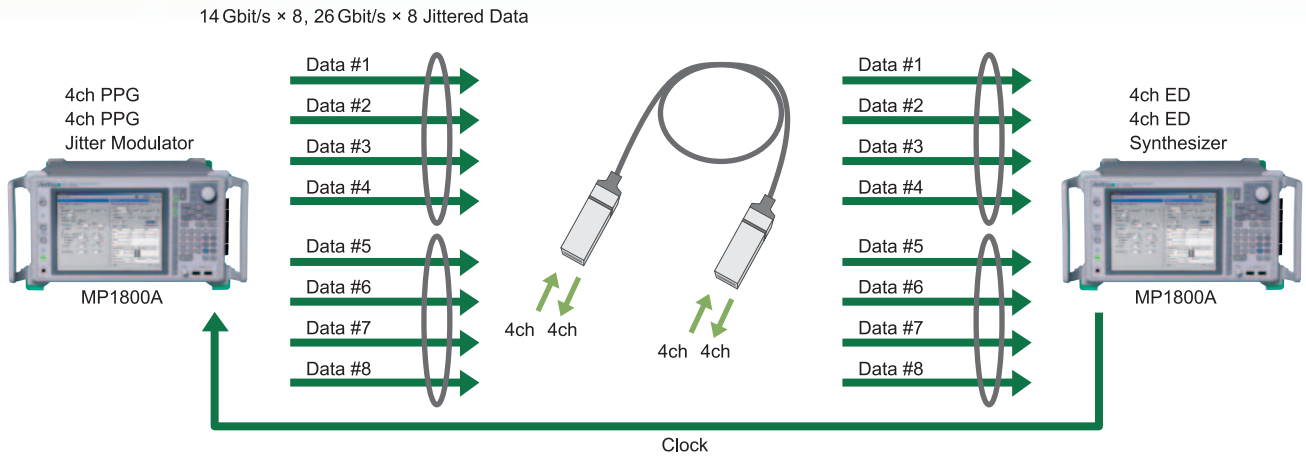
- Each PPG slot can output pre-bias and reset signals for the PON BER test. (Level: H: 0 V, L: –1 V)
- The PON OLT Upstream test can be performed at up to 12.5 Gbit/s using one MP1800A.

Application 3: 28 Gbit/s Band Ultrafast Interconnect Evaluation



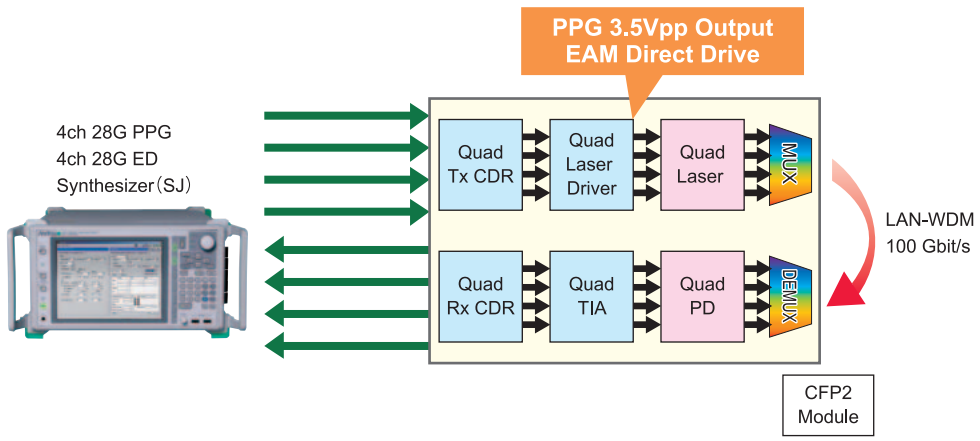
- Jitter tolerance tests using SJ, RJ, BUE-And SSC
- Confirm skew and cross talk effect using channel synchronization and data delay function

Application 4: AOC (Active Optical Cable) Evaluation



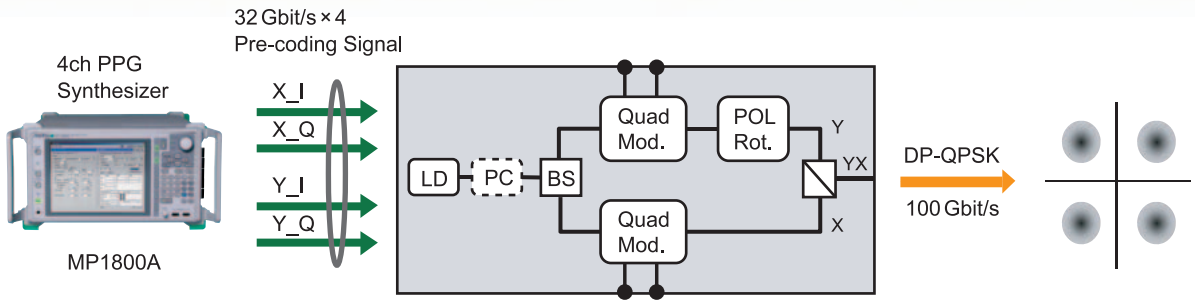
- Simultaneous 8ch (2 × 4ch end-to-end) BER measurement
- Crosstalk test
- Jitter Tolerance test
- Bathtub Jitter, Eye Diagram analysis

Application 5: CFP2/CFP4, EML Device Evaluation



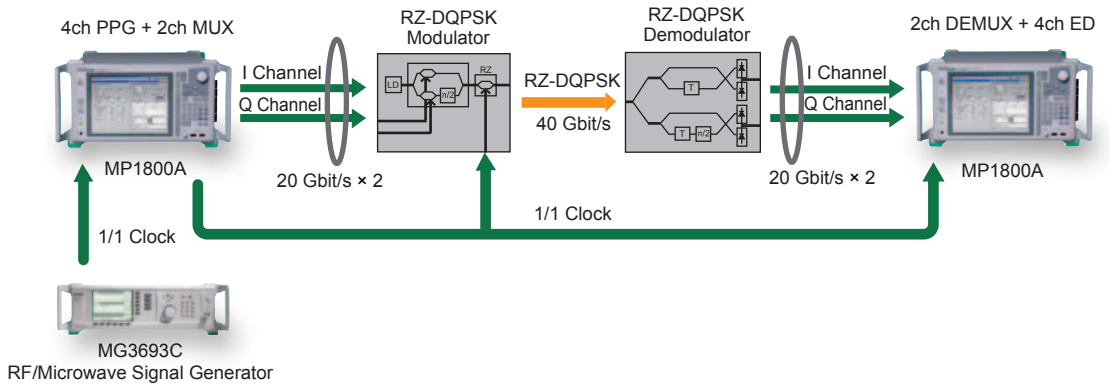
- Simultaneous 4ch BER measurement
- Optical output waveform optimization using cross-point adjustment
- Inter-lane timing and skew control
- High-quality and high-amplitude waveform ideal for EML module evaluation (3.5 Vp-p option)

Application 6: 100 Gbit/s DP-QPSK Evaluation



- Pre-coding signal generator synchronized between channels
- Optical output waveform optimization using cross-point adjustment
- Timing control and skew control between channels
- High-quality and high-amplitude waveform ideal for EML module evaluation (3.5 Vp-p option)

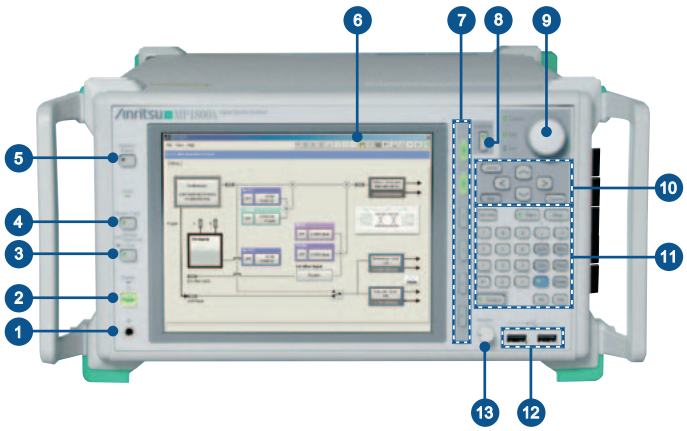
40 Gbit/s Band DQPSK Optical Module/Device Evaluation



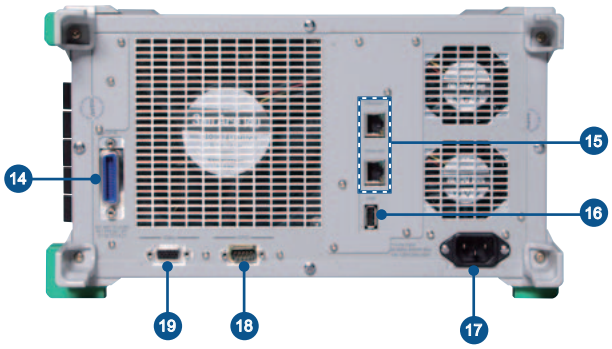
- High-quality and high-amplitude waveform ideal for phase modulator evaluation (3.5 Vp-p option)
- Evaluation using 40 Gbit/s DQPSK precoded signals

Panel Layout

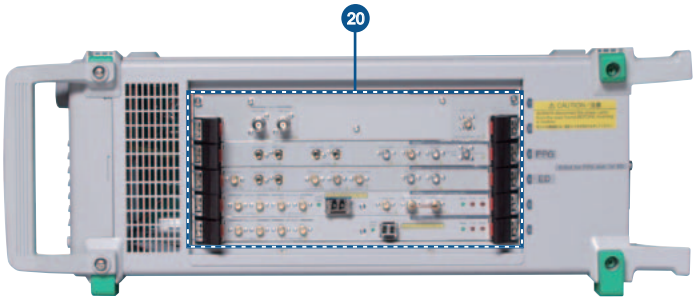
MP1800A Signal Quality Analyzer (6-Slot)



Front



Rear



Side (Right)

1 **Ground**
This terminal is used to discharge static electricity.

2 **Power**

3 **Panel Lock/Remote**
This key locks the panel operation keys.

4 **Screen Copy**
This key copies the currently displayed screen.

5 **System Alarm**
The key LED lights at a system error and a dialog explaining the error contents is displayed.

6 **Display**
8.4-inch Color TFT 800 × 600 pixels

7 **Slot Keys**
These keys correspond to the operation screen for each installed module.

8 **Customize Key**
This key is used to call up to eighteen commonly used screens.

9 **Rotary Encoder**
When the [Edit] key lamp is lit, turning this rotary encoder increases or decreases numeric values. When the [Cursor] key lamp is lit, the operation item can be set. Press the rotary encoder to switch between the [Edit] and [Cursor] functions.

10 **Cursor Key**
These keys move the screen cursor up, down, left and right on screen.

11 **Ten Key**
These ten keys are for inputting numeric values, units, etc.

12 **USB**
Two Rev. 1.1 USB ports

13 **Volume**
This knob increases and decreases the volume of the measurement error alarm.

14 **GPIB**
This connector is used when the MP1800A-001 GPIB option is installed.

15 **Ethernet**
This unit has two RJ45 Ethernet jacks supporting connection to 10 BASE-T or 100 BASE-TX cables.

16 **USB**
Rev. 1.1 USB port

17 **AC Inlet**
This socket is for connecting the 3-wire power cord.

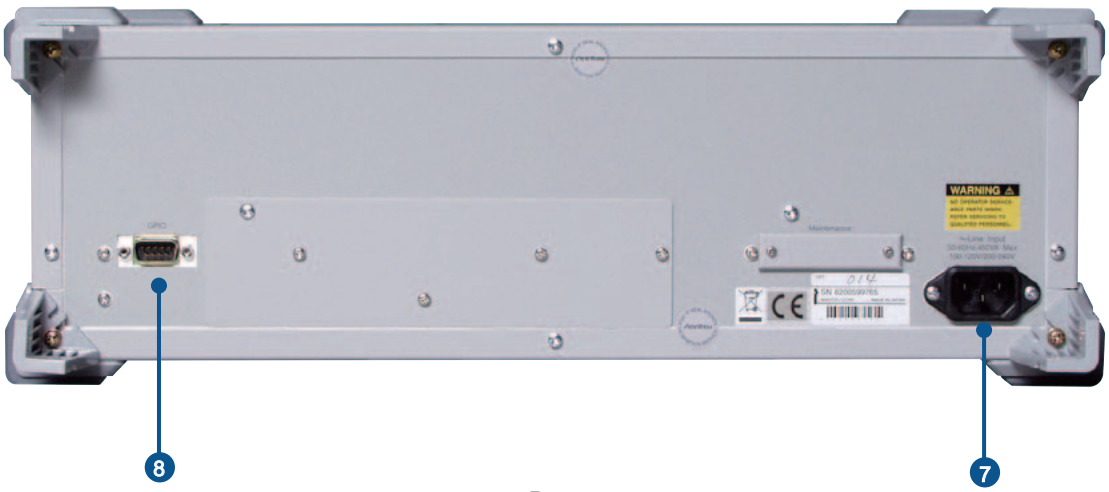
18 **GPIO**
Reserved for future use.

19 **VIDEO**
This connector is for an external display.

20 **Slots for Modules**
These slots are for installing up to six modules.

MT1810A 4Slot Chassis

Front



Rear

1 **Ground**
This terminal is used to discharge static electricity.

2 **Power**

3 **Slots for Modules**
These slots are for installing up to four modules.

4 **Main frame ID**
Used to identify the MT1810A units when one host PC controls multiple (up to 4) MT1810A units.

5 **Volume**
This knob increases and decreases the volume of measurement error alarm.

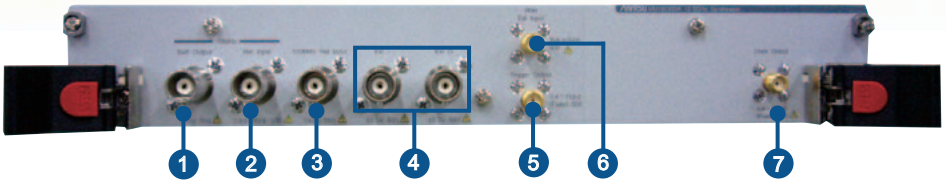
6 **Ethernet**
This unit has two RJ45 Ethernet jacks supporting connection to 10 BASE-T or 100 BASE-TX cables.

7 **AC Inlet**
This socket is for connecting the 3-wire power cord.

8 **GPIO**
Reserved for future use.

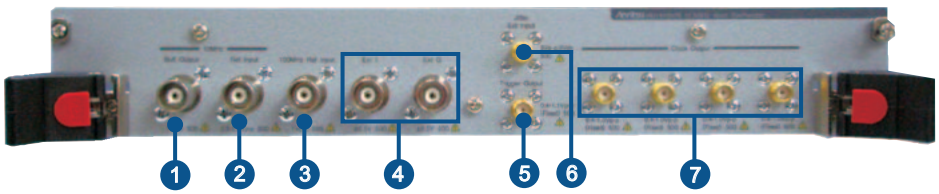
MP1800 Series Modules

• MU181000A 12.5 GHz Synthesizer



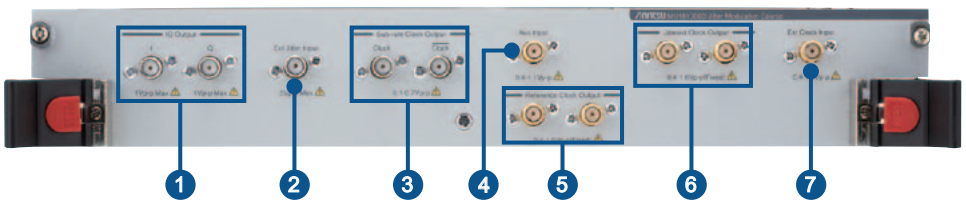
1	10 MHz Buff Output	Output for 10 MHz reference clock	5	Trigger Output*1	Output for 1/64 clock or 1/1 clock
2	10 MHz Ref Input	Input for 10 MHz reference clock			
3	100 MHz Ref Input*1	Input for 100 MHz reference clock	6	Jitter Ext Input*1	Input for jitter modulation signal
4	Ext I, Q*1	Input for I, Q signal	7	Clock Output	Clock output

• MU181000B 12.5 GHz 4 Port Synthesizer



1	10 MHz Buff Output	Output for 10 MHz reference clock	5	Trigger Output*2	Output for 1/64 clock or 1/1 clock
2	10 MHz Ref Input	Input for 10 MHz reference clock			
3	100 MHz Ref Input*2	Input for 100 MHz reference clock	6	Jitter Ext Input*2	Input for jitter modulation signal
4	Ext I, Q*2	Input for I, Q signal	7	Clock Output 1 to 4	Clock output 1 to 4

• MU181500B Jitter Modulation Source



1	IQ Output	Outputs IQ signals	5	Reference Clock Output	Outputs two 1/1, 1/2, or 1/4 frequency-divided clocks based on either of following inputs: • Ext Clock Input • Aux Input
2	Ext Jitter Input	Input for modulation signal source			
3	Sub-rate Clock Output	Outputs frequency-divided clock (1/8 to 1/256) based on either of following inputs: • Ext Clock Input • Aux Input	6	Jittered Clock Output	Outputs two jitter-modulated clock signals
4	Aux Input	Input clock signals	7	Ext Clock Input	Input for external clock

• MU181800A 12.5 GHz Clock Distributor

1	Clock Output 1 to 4	Output for divided clock of Clock Input	2	Clock Input	Clock input

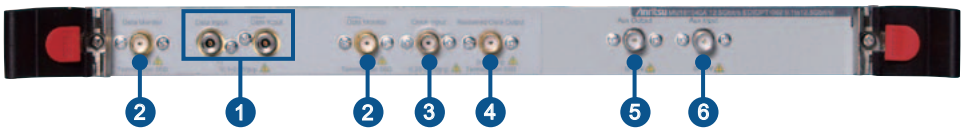
• MU181800B 14 GHz Clock Distributor

1	Clock Output 1 to 5	Outputs for divided clock of Clock Input	2	Clock Input	Clock input

• MU181020A 12.5 Gbit/s PPG/MU181020B 14 Gbit/s PPG

1	Data/$\overline{\text{Data}}$ Output	Output for differential data signal	4	Aux Output	Output for auxiliary signal
2	Clock/$\overline{\text{Clock}}$ Output*3	Output for differential clock signal	5	Aux Input	Input for auxiliary signal
3	Gating Output	Output for burst timing signal	6	Ext. Clock Input	Clock input

• MU181040A 12.5 Gbit/s ED/MU181040B 14 Gbit/s ED

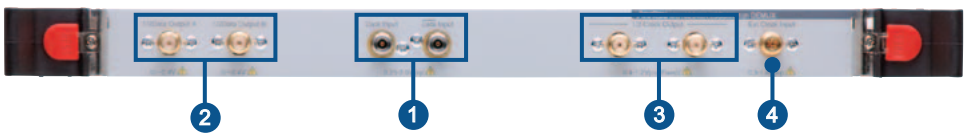


1	Data/$\overline{\text{Data}}$ Input	Input for differential data signal	4	Recovered Clock Output*5	Output for regenerated clock from input data
2	Data/$\overline{\text{Data}}$ Monitor*4	Output for divided clock of input data	5	Aux Output	Output for auxiliary signal
3	Clock Input*4	Clock input	6	Aux Input	Input for auxiliary signal

• MU182020A 25 Gbit/s 1ch MUX

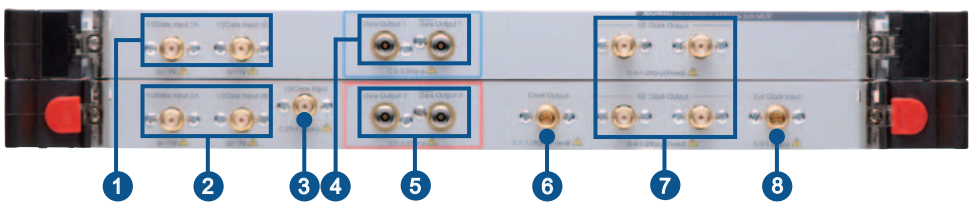
1	1/2 Data Input A/B	Input for two data signals from MU181020A/B	4	Clock Output	Clock output
2	1/2 Clock Input	Input for clock signal from MU181020A/B	5	1/2 Clock Output	Output for two clock signals to MU181020A/B
3	Data/$\overline{\text{Data}}$ Output	Output for 2/1 multiplexed differential data signal	6	Ext. Clock Input	System clock input

• MU182040A 25 Gbit/s 1ch DEMUX



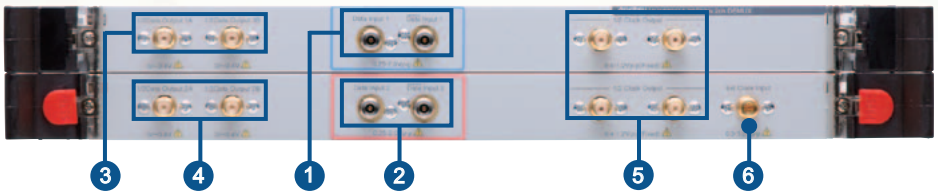
1	Data/$\overline{\text{Data}}$ Input	Differential data input	3	1/2 Clock Output	Output for 1/2 clock
2	1/2 Data Output A/B	Output for 1/2 demultiplexed input signal	4	Ext. Clock Input	Clock input

• MU182021A 25 Gbit/s 2ch MUX



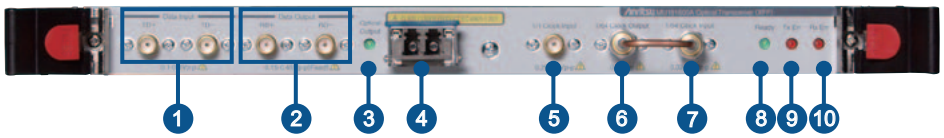
1	1/2 Data Input 1A/1B	Input for two data signals from MU181020A/B	5	Data/$\overline{\text{Data}}$ Output 2	Output for 2/1 multiplexed differential data signal
2	1/2 Data Input 2A/2B	Input for two data signals from MU181020A/B	6	Clock/$\overline{\text{Clock}}$ Output*6	Clock output
3	1/2 Clock Input	Input for clock signal from MU181020A/B	7	1/2 Clock Output	Output for four clock signals to MU181020A/B
4	Data/$\overline{\text{Data}}$ Output 1	Output for 2/1 multiplexed differential data signal	8	Ext. Clock Input	System clock input

• MU182041A 25 Gbit/s 2ch DEMUX



1	Data/$\overline{\text{Data}}$ Input 1	Differential data input	4	1/2 Data Output 2A/2B	Output for 2/1 demultiplexed input signal
2	Data/$\overline{\text{Data}}$ Input 2	Differential data input	5	1/2 Clock Output	Output for 2/1 clock
3	1/2 Data Output 1A/1B	Output for 2/1 demultiplexed input signal	6	Ext. Clock Input	Clock input

• MU181600A Optical Transceiver (XFP)

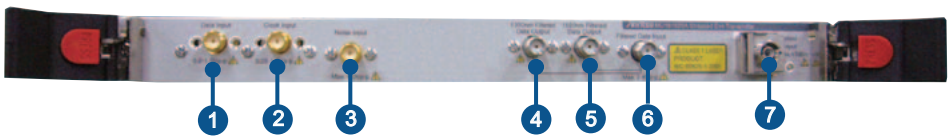


1	TD+/TD– Data Input	Input for electrical signal to XFP module	6	1/64 Clock Output	Output for 1/64 clock of 1/1 clock input
2	RD+/RD– Data Output	Output for electrical signal output from XFP module	7	1/64 Clock Input	Input for 1/64 reference clock
3	Optical Output (LED)	Displays XFP module optical signal status	8	Ready (LED)	Displays XFP module installation status
4	Slot for Module	Slot for XFP module	9	Tx Err (LED)	Displays XFP transmitter error status
5	1/1 Clock Input	Input for 1/1 clock	10	Rx Err (LED)	Displays XFP receiver error status

• MU181601A Optical Transceiver (SFP)

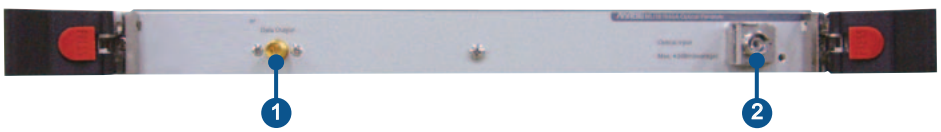
1	TD+/TD– Data Input	Input for electrical signal to SFP module	5	Ready (LED)	Displays SFP module installation status
2	RD+/RD– Data Output	Output for electrical signal output from SFP module	6	Tx Err (LED)	Displays SFP transmitter error status
3	Optical Output (LED)	Displays SFP module optical signal status	7	Rx Err (LED)	Displays SFP receiver error status
4	Slot for Module	Slot for SFP module			

• MU181620A Stressed Eye Transmitter



1	Data Input	Input for data signal	5	1550 nm Filtered Data Output*8	Output for stressed electrical data for 1550 nm
2	Clock Input	Clock input			
3	Noise Input	Input for noise signal for stressed signal	6	Filtered Data Input*9	Input for stressed electrical data Connect 1310 nm or 1550 nm Filtered Data Output
4	1310 nm Filtered Data Output*7	Output for stressed electrical data for 1310 nm	7	Optical Output	Output for optical data

• MU181640A Optical Receiver

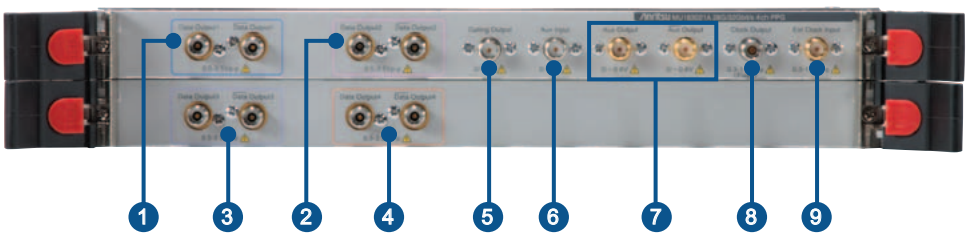


1	Data Output	Data output	2	Optical Input	Input for optical signal

• **MU183020A 28G/32G bit/s PPG (1ch or 2ch)**

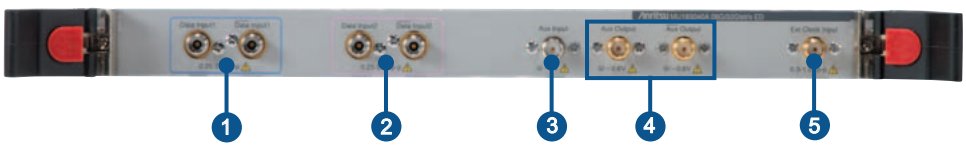
1	Data1/XData1 Output*10	Output for Ch1 differential data signal	5	Aux/XAux Output	Output for differential auxiliary signal
2	Data2/XData2 Output*11	Output for Ch2 differential data signal	6	Clock Output	Output for clock signal
3	Gating Output	Output for burst timing signal	7	Ext Clock Input	Input for external clock signal
4	Aux Input	Input for auxiliary signal			

• **MU183021A 28G/32G bit/s 4ch PPG**



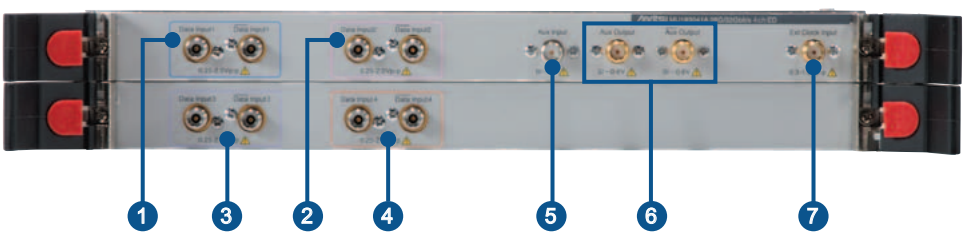
1	Data1/XData1 Output	Output for Ch1 differential data signal	6	Aux Input	Input for auxiliary signal
2	Data2/XData2 Output	Output for Ch2 differential data signal	7	Aux/XAux Output	Output for differential auxiliary signal
3	Data3/XData3 Output	Output for Ch3 differential data signal	8	Clock Output	Output for clock signal
4	Data4/XData4 Output	Output for Ch4 differential data signal	9	Ext Clock Input	Input for external clock signal
5	Gating Output	Output for burst timing signal			

• **MU183040A 28G/32G bit/s ED (1ch or 2ch)**



1	Data1/XData1 Input*10	Input for Ch1 differential data signal	4	Aux/XAux Output	Output for differential auxiliary signal
2	Data2/XData2 Input*11	Input for Ch2 differential data signal	5	Ext Clock Input	Input for external clock signal
3	Aux Input	Input for auxiliary signal			

• **MU183041A 28G/32G bit/s 4ch ED**



1	Data1/XData1 Input	Input for Ch1 differential data signal	5	Aux Input	Input for auxiliary signal
2	Data2/XData2 Input	Input for Ch2 differential data signal	6	Aux/XAux Output	Output for differential auxiliary signal
3	Data3/XData3 Input	Input for Ch3 differential data signal	7	Ext Clock Input	Input for external clock signal
4	Data4/XData4 Input	Input for Ch4 differential data signal			

∗1: Only enabled when Jitter Modulation option (MU181000A-001) installed
∗2: Only enabled when Jitter Modulation option (MU181000B-001) installed
∗3: Single-end outputs without Differential Clock output option (MU181020A/B-021, 121)
∗4: Only enabled when 0.1 Gbit/s to 12.5 Gbit/s option (MU181040A-002) or 0.1 Gbit/s to 14 Gbit/s option (MU181040B-002) installed
∗5: Only enabled when MU181040A/B-020/120 installed
∗6: Single-end output without Differential Clock Output option (MU182020A-021)
∗7: Only enabled when MU181620A-011/013 installed
∗8: Only enabled when MU181620A-012/013 installed
∗9: Only enabled when MU181620A-011/012/013 installed
∗10: Data/XData when 1ch option was selected.
∗11: Not implemented when 1ch option was selected.

Specifications

● MP1800A Signal Quality Analyzer

LCD Display	8.4-inch Color TFT, 800 × 600 pixels
Peripheral Interface	VGA out (SVGA), USB 1.1 (3 Ports)
Remote Interface	GPIB [MP1800A-001], LAN (2 ports) [MP1800A-002]
Options	2-slot PPG and/or ED [MP1800A-014], 4-slot PPG and/or ED [MP1800A-015], 6-slot PPG and/or ED [MP1800A-016]
Power Supply	100 V (ac) to 120 V (ac) / 200 V (ac) to 240 V (ac) [auto-switching between 100 V (ac) / 200 V (ac)], 47.5 Hz to 63 Hz
Power Consumption	≤600 VA
Operating Temperature	5° to 40°C
Dimensions and Mass	320 mm (W) × 177 mm (H) × 450 mm (D), ≤13 kg (without modules)
EMC	EN61326-1, EN61000-3-2
LVD	EN61010-1

● MT1810A 4Slot Chassis

Remote Interface	LAN (2 ports)
Options	2-slot PPG and/or ED [MT1810A-014], 4-slot PPG and/or ED [MT1810A-015]
Power Supply	100 V (ac) to 120 V (ac) / 200 V (ac) to 240 V (ac) [auto-switching between 100 V (ac) / 200 V (ac)], 47.5 Hz to 63 Hz
Power Consumption	≤450 VA
Operating Temperature	5° to 40°C
Dimensions and Mass	350 mm (W) × 132.5 mm (H) × 400 mm (D), ≤13 kg (without modules)
EMC	EN61326-1, EN61000-3-2
LVD	EN61010-1

● MU181000A 12.5 GHz Synthesizer/MU181000B 12.5 GHz 4port Synthesizer

Clock Output	Number of Output: 1 [MU181000A], 4 [MU181000B] Frequency Range: 0.1 GHz to 12.5 GHz, Steps: 1 kHz/1 MHz Offset from Set Frequency: –1000 ppm to +1000 ppm, Steps: 1 ppm, 1 Hz (Min) Level: 0.632 Vp-p to 2 Vp-p (AC) [MU181000A], 0.4 Vp-p to 1 Vp-p (AC) [MU181000B, MU181000A/B-001] SSB Phase Noise: ≤–80 dBc/Hz (10 kHz offset) Intrinsic Jitter: ≤20 ps p-p [MU181000A/B] ≤20 ps p-p (fc>400 MHz) [MU181000A/B-001] Waveform: Square wave (<1 GHz), Square wave or Sine wave (≥1 GHz) Duty: 50±10% Inter-channel Skew: ≤10 ps (12.5 GHz) [MU181000B] Connector: SMA(f.), Termination: 50Ω/GND
10 MHz Input	Frequency: 10 MHz ±10 ppm Level: 0.5 Vp-p to 2.0 Vp-p Waveform: Square wave or Sine wave Duty: 50±10% Connector: BNC, Termination: 50Ω/GND
10 MHz Output	Level: 1.0 Vp-p ±30% (AC) Waveform: Square wave Duty: 50±10% Connector: BNC, Termination: 50Ω/GND

● MU181000A/B-001 Jitter Modulation

External Modulation Input

Frequency Range: 9 Hz to 1 GHz
Level Range: 3 Vp-p, 0 V (dc) (Max.)
Waveform: Sine wave
Connector: SMA(f.), Termination: 50Ω/GND

External I, Q Input

Frequency Range: DC to 320 MHz (–3 dB)
Bandwidth Limit: 5 MHz (0.1 GHz≤fc≤0.4 GHz), 10 MHz (0.4 GHz<fc≤0.65 GHz), 20 MHz (0.65 GHz<fc≤1.4 GHz), 100 MHz (1.4 GHz<fc≤2.4 GHz), 320 MHz (2.4 GHz<fc≤4.0 GHz)
Level Range: ±0.5 V
Connector: BNC, Termination: 50Ω/GND

100 MHz Reference Signal Input (SSC)

Output Center Frequency is × 25 or × 50 of Reference Input Frequency
Modulation Frequency: 30 kHz to 33 kHz
Frequency Deviation: 50 kHz
Level: 1.0 Vp-p ±30% (AC)
Waveform: Square wave or Sine wave
Duty: 50±10%
Connector: BNC, Termination: 50Ω/GND

Trigger Output

Available from 800 MHz to 12.5 GHz of center frequency (fc)
Frequency: 1/64 (800 MHz<fc≤6.4 GHz), 1/1 or 1/64 selectable (6.4 GHz<fc≤12.5 GHz)
Level: 0.4 Vp-p to 1.1 Vp-p (AC)
Connector: SMA(f.), Termination: 50Ω/GND

Internal Jitter Function

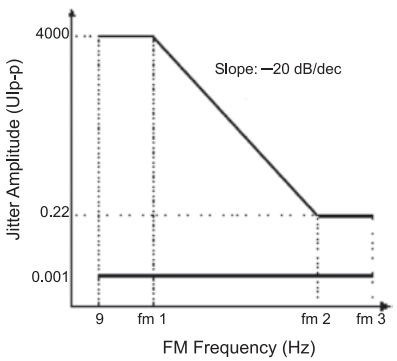
Modulation Frequency Range

Center Frequency (fc)	fm1	fm2	fm3
0.1 GHz to 0.8 GHz	13.75 Hz	250 kHz	5 MHz
0.8 GHz to 1.6 GHz	27.5 Hz	500 kHz	10 MHz
1.6 GHz to 3.2 GHz	55 Hz	1 MHz	20 MHz
3.2 GHz to 6.4 GHz	110 Hz	2 MHz	40 MHz
6.4 GHz to 12.5 GHz	220 Hz	4 MHz	80 MHz

Modulation Frequency Accuracy: ±100 ppm
Jitter Amplitude Accuracy[*1]:
±0.01 UI±Q% (0.001 UIp-p to 2.19 UIp-p, fc<1 GHz)
±0.02 UI±Q% (0.001 UIp-p to 2.19 UIp-p, fc≥1 GHz)
±0.2 UI±Q% (2.2 UIp-p to 21.99 UIp-p)
±2 UI±Q% (22 UIp-p to 4000 UIp-p)

FM	Q
9 Hz≤fm≤500 kHz	7
500 kHz<fm≤2 MHz	12
2 MHz<fm≤80 MHz	15

Jitter Mask[*1]



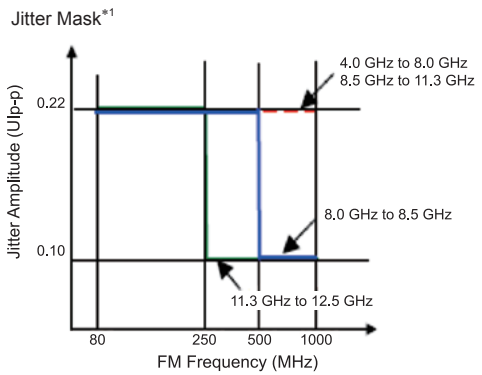
External Jitter Function

Modulation Frequency Range:
9 Hz to 5 MHz (0.1 GHz≤fc≤0.4 GHz)
9 Hz to 10 MHz (0.4 GHz<fc≤0.65 GHz)
9 Hz to 20 MHz (0.65 GHz<fc≤1.4 GHz)
9 Hz to 100 MHz (1.4 GHz<fc≤2.4 GHz)
9 Hz to 500 MHz (2.4 GHz<fc≤4.0 GHz)
9 Hz to 1 GHz (4.0 GHz<fc≤12.5 GHz)
UI Range: 0.22, 2.0, 20, 200, 4000 UI

Modulation Frequency Range[*1]

Center Frequency	Input Frequency	Jitter Amplitude
1.4 GHz to 2.4 GHz	80 MHz to 100 MHz	Max. 0.22 UI
2.4 GHz to 4.0 GHz	80 MHz to 500 MHz	
4.0 GHz to 8.0 GHz	80 MHz to 1 GHz	
8.0 GHz to 8.5 GHz	80 MHz to 500 MHz	
	500 MHz to 1 GHz	Max. 0.10 UI
8.5 GHz to 11.3 GHz	80 MHz to 1 GHz	Max. 0.22 UI
11.3 GHz to 12.5 GHz	80 MHz to 250 MHz	Max. 0.22 UI
	250 MHz to 1 GHz	Max. 0.10 UI

Jitter Mask[*1]



Modulation Sensitivity: 0.22 UI Range, Input level: 0.5 Vp-p

Output Clock Frequency	FM Frequency	Input Frequency	Jitter Amplitude
0.1 GHz≤fc≤12.5 GHz	4 MHz	9 Hz to 4 MHz	0.1 UIp-p±0.03 UI
	80 MHz	4 MHz to 80 MHz	
	500 MHz	80 MHz to 500 MHz	
2.4 GHz<fc≤12.5 GHz	1 GHz	500 MHz to 1 GHz	

External Jitter Function

Modulation Sensitivity: 2, 20, 200, 4000 UI Range, Input level: 0.5 Vp-p

Clock Frequency: 0.1 GHz≤fc≤0.8 GHz

Jitter Amplitude	FM Frequency	Input Frequency	Jitter Amplitude
2 UI	250 kHz	27.5 kHz	1 UIp-p±0.3 UI
20 UI	27.5 kHz	2.75 kHz	10 UIp-p±3 UI
200 UI	2.75 kHz	275 Hz	100 UIp-p±30 UI
4000 UI	275 Hz	13.75 Hz	1000 UIp-p±300 UI

Clock Frequency: 0.8 GHz<fc≤1.6 GHz

Jitter Amplitude	FM Frequency	Input Frequency	Jitter Amplitude
2 UI	500 kHz	55 kHz	1 UIp-p±0.3 UI
20 UI	55 kHz	5.5 kHz	10 UIp-p±3 UI
200 UI	5.5 kHz	550 Hz	100 UIp-p±30 UI
4000 UI	550 Hz	27.5 Hz	1000 UIp-p±300 UI

Clock Frequency: 1.6 GHz<fc≤3.2 GHz

Jitter Amplitude	FM Frequency	Input Frequency	Jitter Amplitude
2 UI	1 MHz	110 kHz	1 UIp-p±0.3 UI
20 UI	110 kHz	11 kHz	10 UIp-p±3 UI
200 UI	11 kHz	1.1 kHz	100 UIp-p±30 UI
4000 UI	1.1 kHz	55 Hz	1000 UIp-p±300 UI

Clock Frequency: 3.2 GHz<fc≤6.4 GHz

Jitter Amplitude	FM Frequency	Input Frequency	Jitter Amplitude
2 UI	2 MHz	220 kHz	1 UIp-p±0.3 UI
20 UI	220 kHz	22 kHz	10 UIp-p±3 UI
200 UI	22 kHz	2.2 kHz	100 UIp-p±30 UI
4000 UI	2.2 kHz	110 Hz	1000 UIp-p±300 UI

Clock Frequency: 6.4 GHz<fc≤12.5 GHz

Jitter Amplitude	FM Frequency	Input Frequency	Jitter Amplitude
2 UI	4 MHz	440 kHz	1 UIp-p±0.3 UI
20 UI	440 kHz	44 kHz	10 UIp-p±3 UI
200 UI	44 kHz	4.4 kHz	100 UIp-p±30 UI
4000 UI	4.4 kHz	220 Hz	1000 UIp-p±300 UI

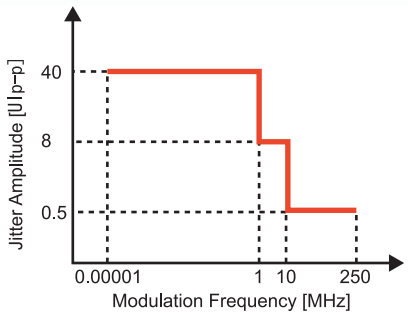
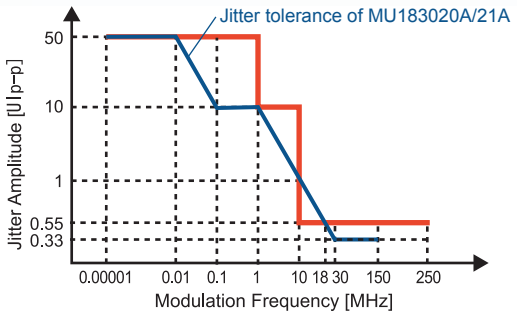
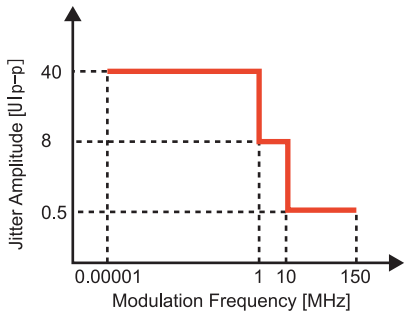
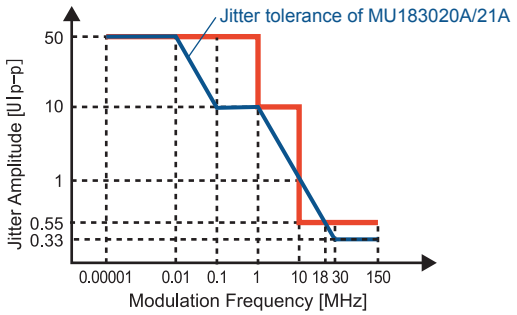
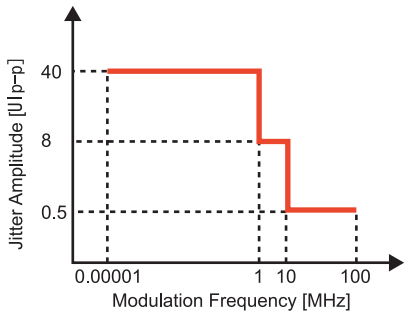
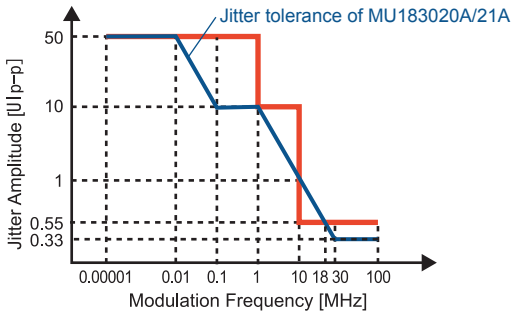
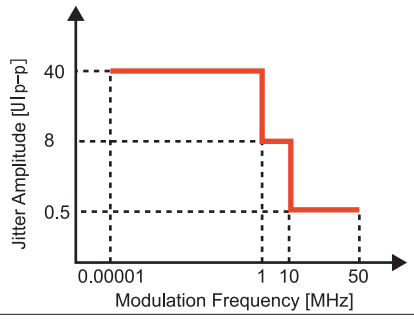
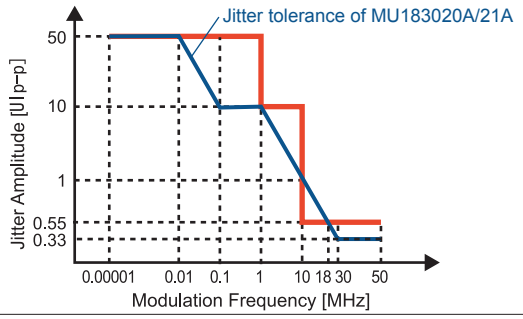
Triangle Wave Modulation

PCIe-Gen I (2.5 GHz) or PCIe-Gen II (5 GHz)
Clock Output Frequency Setting: Spread Method Center/Spread Method Down selectable
Frequency Offset: –1000 ppm to +1000 ppm, Steps: 1 ppm
Modulation Frequency Accuracy: 31.25 kHz ±1000 ppm
Frequency Deviation: ±6.25 MHz (PCIe-Gen I, 2.5 GHz), ±12.5 MHz (PCIe-Gen II, 5 GHz)
Deviation Accuracy: ±10%

∗1: The maximum jitter amplitude is limited according to the jitter tolerance of PPG or ED modules. Refer to the jitter tolerance specification of PPG/ED modules.

● MU181500B Jitter Modulation Source

External Clock Input	Number of Input: 1 Frequency Range: 6.400 001 GHz to 12.500 000 GHz (MU181000A/B, Combination: On) 0.800 000 GHz to 15.000 000 GHz (MU181000A/B, Combination: Off, or External synthesizer) Amplitude: 0.4 Vp-p to 1.0 Vp-p Connector: SMA(f.), Termination: 50Ω/AC Coupling
External Jitter Input	Number of Input: 1 Frequency Range: 10 kHz to 1 GHz Amplitude: 0 to 2.0 Vp-p Connector: SMA(f.), Termination: 50Ω/GND
Jittered Clock Output	Number of Output: 2 Frequency Range: 0.800 001 GHz to 1.562 500 GHz (MU181000A/B, Combination: On), Steps: 0.000 001 GHz 1.600 001 GHz to 3.125 000 GHz (MU181000A/B, Combination: On), Steps: 0.000 001 GHz 3.200 001 GHz to 6.250 000 GHz (MU181000A/B, Combination: On), Steps: 0.000 001 GHz 6.400 001 GHz to 12.500 000 GHz (MU181000A/B, Combination: On), Steps: 0.000 001 GHz 12.800 002 GHz to 15.000 000 GHz (MU181000A/B, Combination: On), Steps: 0.000 002 GHz 0.8 GHz to 15 GHz (MU181000A/B, Combination: Off, or External synthesizer) Frequency Offset: –1000 ppm to +1000 ppm (MU181000A/B, Combination: On), Steps: 1 ppm None (MU181000A/B, Combination: Off, or External synthesizer) Amplitude: 0.4 Vp-p (Min.), 1.0 Vp-p (Max.) Intrinsic Jitter: ≤350 fs (4.25, 7.0125, 10, 12.5, 14, 15 GHz) Connector: SMA(f.), Termination: 50Ω/AC Coupling
IQ Output	Number of Output: 2 (I, Q) Amplitude: 1 Vp-p (Max.) Connector: SMA(f.), Termination: 50Ω/GND
AUX Input	Number of Input: 1 Frequency Range: Same frequency with External Clock Input Amplitude: 0.4 Vp-p (Min.), 1.1 Vp-p (Max.) Connector: SMA(f.), Termination: 50Ω/AC Coupling
Reference Clock Output	Number of Output: 2 Reference Clock: External Clock Input or AUX Input (MU181000A/B, Combination: On) External Clock Input (MU181000A/B, Combination: Off, or External synthesizer) Frequency Range: 1/N of Jittered Clock Output Frequency (N: 1, 2, or 4) Amplitude: 0.4 Vp-p (Min.), 1.0 Vp-p (Max.) (Jittered Clock Output Frequency: ≥4 GHz) 0.4 Vp-p (Min.), 1.2 Vp-p (Max.) (Jittered Clock Output Frequency: <4 GHz) Connector: SMA(f.), Termination: 50Ω/AC Coupling
Sub-rate Clock Output	Number of Output: 2 (Differential) Frequency Range: 1/N of Jittered Clock Output Frequency (N: 8 to 256, Steps: 1) Amplitude: 0.1 Vp-p to 0.7 Vp-p, Steps: 10 mV Accuracy: ±70 mV ±20% of Amplitude (N: 8) Connector: SMA(f.), Termination: 50Ω/AC Coupling

Internal Sinusoidal Jitter (SJ1)	Mask[*1] Jittered Clock Output Frequency: 8.500 001 GHz to 15 GHz Full Rate Mode[*2]  Half Rate Mode[*2]  Jittered Clock Output Frequency: 4.000 001 GHz to 8.5 GHz Full Rate Mode[*2]  Half Rate Mode[*2]  Jittered Clock Output Frequency: 1.200 001 GHz to 4 GHz Full Rate Mode[*2]  Half Rate Mode[*2]  Jittered Clock Output Frequency: 0.800 001 GHz to 1.2 GHz Full Rate Mode[*2]  Half Rate Mode[*2] 

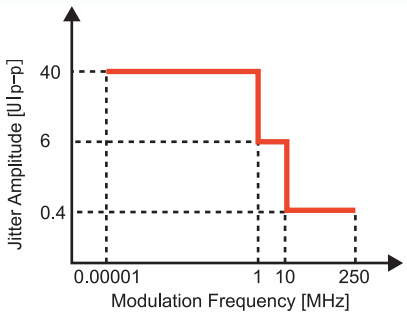
Internal Sinusoidal Jitter (SJ1)	Modulation Frequency (FM): 10 Hz to 10 kHz, Steps: 1 Hz 10 kHz to 100 kHz, Steps: 10 Hz 100 kHz to 1 MHz, Steps: 100 Hz 1 MHz to 10 MHz, Steps: 1 kHz 10 MHz to 100 MHz, Steps: 10 kHz 100 MHz to 250 MHz, Steps: 100 kHz Accuracy: ±100 ppm Amplitude[*1]: Full Rate Mode[*2] Jittered Clock Output Frequency: 8.500 001 GHz to 15 GHz 0 to 40 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.1 UI 0 to 8 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI 0 to 0.5 UIp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.001 UI Jittered Clock Output Frequency: 4.000 001 GHz to 8.5 GHz 0 to 40 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.1 UI 0 to 8 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI 0 to 0.5 UIp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.001 UI Jittered Clock Output Frequency: 1.200 001 GHz to 4 GHz 0 to 40 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.1 UI 0 to 8 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI 0 to 0.5 UIp-p (FM: 10.01 MHz to 100 MHz), Steps: 0.001 UI Jittered Clock Output Frequency: 1.800 001 GHz to 1.2 GHz 0 to 40 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.1 UI 0 to 8 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI 0 to 0.5 UIp-p (FM: 10.01 MHz to 50 MHz), Steps: 0.001 UI Half Rate Mode[*2] Jittered Clock Output Frequency: 8.500 001 GHz to 15 GHz 0 to 50 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI 0 to 10 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI 0 to 0.55 UIp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.002 UI Jittered Clock Output Frequency: 4.000 001 GHz to 8.5 GHz 0 to 50 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI 0 to 10 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI 0 to 0.55 UIp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.002 UI Jittered Clock Output Frequency: 1.200 001 GHz to 4 GHz 0 to 50 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI 0 to 10 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI 0 to 0.55 UIp-p (FM: 10.01 MHz to 100 MHz), Steps: 0.002 UI Jittered Clock Output Frequency: 1.800 001 GHz to 1.2 GHz 0 to 50 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI 0 to 10 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI 0 to 0.55 UIp-p (FM: 10.01 MHz to 50 MHz), Steps: 0.002 UI Accuracy: ±0.03 UI ±Q% (Amplitude: 0.002 UIp-p to 2.19 UIp-p) ±0.2 UI ±Q% (Amplitude: 2.2 UIp-p to 21.9 UIp-p) ±2 UI ±Q% (Amplitude: 22 UIp-p to 50 UIp-p) <table><tr><th>FM</th><th>Q</th></tr><tr><td>10 Hz≤fm≤500 kHz</td><td>7</td></tr><tr><td>500 kHz<fm≤2 MHz</td><td>10</td></tr><tr><td>2 MHz<fm≤80 MHz</td><td>13</td></tr><tr><td>80 MHz<fm≤250 MHz</td><td>15</td></tr></table>On/Off Function: Supported

External Sinusoidal Jitter (SJ2)
[MU181000A/B-001]

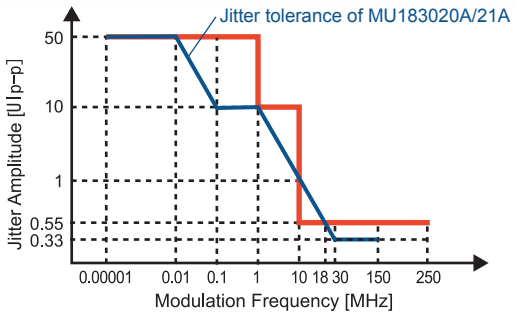
Mask[*1]

Jittered Clock Output Frequency: 6.400 001 GHz to 15 GHz

Full Rate Mode[*2]

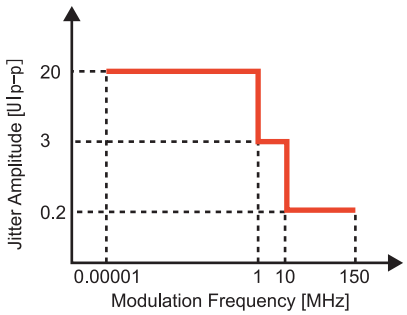


Half Rate Mode[*2]

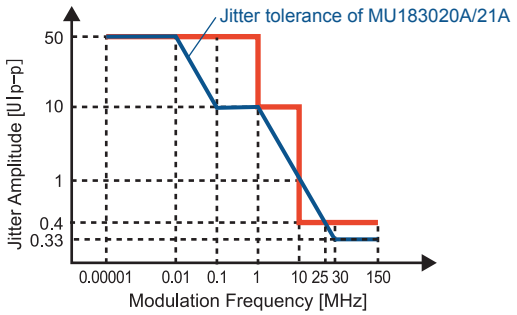


Jittered Clock Output Frequency: 3.200 001 GHz to 6.25 GHz

Full Rate Mode[*2]

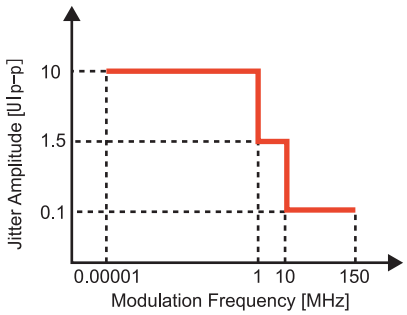


Half Rate Mode[*2]

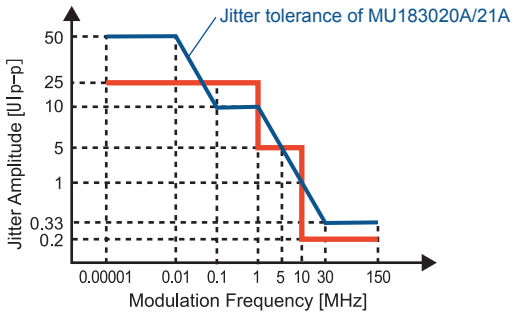


Jittered Clock Output Frequency: 1.800 001 GHz to 3.125 GHz

Full Rate Mode[*2]

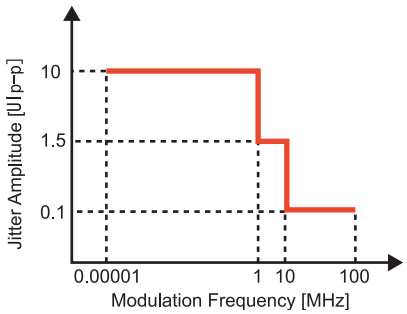


Half Rate Mode[*2]

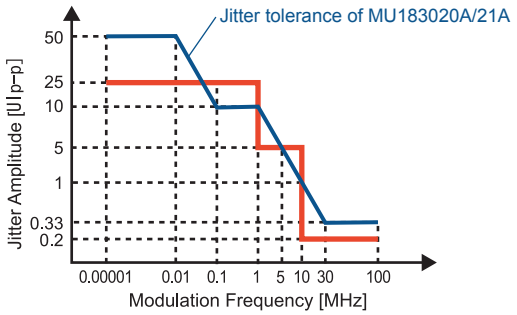


Jittered Clock Output Frequency: 1.600 001 GHz to 1.8 GHz

Full Rate Mode[*2]

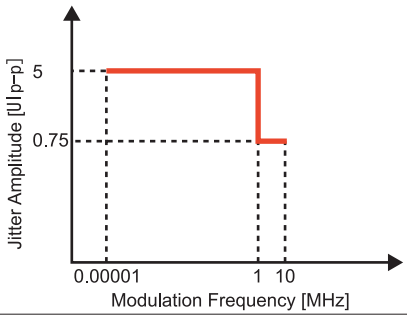


Half Rate Mode[*2]

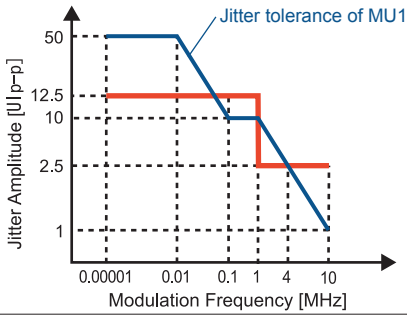


Jittered Clock Output Frequency: 0.800 001 GHz to 1.562 5 GHz

Full Rate Mode[*2]



Half Rate Mode[*2]



<table>
<tr>
<td>External Sinusoidal Jitter (SJ2)
[MU181000A/B-001]</td>
<td>
Modulation Frequency (FM): 10 Hz to 10 kHz, Steps: 1 Hz
10 kHz to 100 kHz, Steps: 10 Hz
100 kHz to 1 MHz, Steps: 100 Hz
1 MHz to 10 MHz, Steps: 1 kHz
10 MHz to 100 MHz, Steps: 10 kHz
100 MHz to 250 MHz, Steps: 100 kHz
Accuracy: ±100 ppm
Amplitude*1:
Full Rate Mode*2
Jittered Clock Output Frequency: 6.400 001 GHz to 15 GHz
0 to 40 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.1 UI
0 to 6 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
0 to 0.4 UIp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.001 UI
Jittered Clock Output Frequency: 3.200 001 GHz to 6.25 GHz
0 to 20 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.1 UI
0 to 3 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
0 to 0.2 UIp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.001 UI
Jittered Clock Output Frequency: 1.800 001 GHz to 3.125 GHz
0 to 10 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.1 UI
0 to 1.5 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
0 to 0.1 UIp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.001 UI
Jittered Clock Output Frequency: 1.600 001 GHz to 1.8 GHz
0 to 10 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.1 UI
0 to 1.5 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
0 to 0.1 UIp-p (FM: 10.01 MHz to 100 MHz), Steps: 0.001 UI
Jittered Clock Output Frequency: 0.800 001 GHz to 1.562 5 GHz
0 to 5 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.1 UI
0 to 0.75 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
Half Rate Mode*2
Jittered Clock Output Frequency: 6.400 001 GHz to 15 GHz
0 to 50 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
0 to 10 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
0 to 0.55 UIp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.002 UI
Jittered Clock Output Frequency: 3.200 001 GHz to 6.25 GHz
0 to 50 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
0 to 10 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
0 to 0.4 UIp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.002 UI
Jittered Clock Output Frequency: 1.800 001 GHz to 3.125 GHz
0 to 25 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
0 to 5 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
0 to 0.2 UIp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.002 UI
Jittered Clock Output Frequency: 1.600 001 GHz to 1.8 GHz
0 to 25 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
0 to 5 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
0 to 0.2 UIp-p (FM: 10.01 MHz to 100 MHz), Steps: 0.002 UI
Jittered Clock Output Frequency: 0.800 001 GHz to 1.562 5 GHz
0 to 12.5 UIp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
0 to 2.5 UIp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
Accuracy: ±0.03 UI ±Q% (Amplitude: 0.002 UIp-p to 2.19 UIp-p)
±0.2 UI ±Q% (Amplitude: 2.2 UIp-p to 21.9 UIp-p)
±2 UI ±Q% (Amplitude: 22 UIp-p to 50 UIp-p)
<table>
<tr><th>FM</th><th>Q</th></tr>
<tr><td>10 Hz≤fm≤500 kHz</td><td>10</td></tr>
<tr><td>500 kHz<fm≤2 MHz</td><td>13</td></tr>
<tr><td>2 MHz<fm≤80 MHz</td><td>15</td></tr>
<tr><td>80 MHz<fm≤250 MHz</td><td>18</td></tr>
</table>
On/Off Function: Supported
</td>
</tr>
<tr>
<td>Spread Spectrum Clocking
(SSC)</td>
<td>
Type: Down-Spread, Center-Spread, Up-Spread
Modulation Frequency: 28 kHz to 34 kHz, Steps: 1 Hz
Accuracy: ±100 ppm
Deviation: 0 to 5000 ppm, Steps: 1 ppm
On/Off Function: Supported
</td>
</tr>
</table>

<table>
<tr><td>Random Jitter (RJ)</td><td>
Bandwidth: 10 kHz to 1 GHz
Crest Factor: 16 dB
Filter Type
User Filter
Filter: 10 MHz, 20 MHz, Through (HPF 3 dB bandwidth)
100 MHz, Through (LPF 3 dB bandwidth)
Amplitude*1:
Full Rate Mode*2
<table>
<tr><th>Jittered Clock Output Frequency [GHz]</th><th>Setting Range [UIp-p]</th><th>Steps [mUI]</th></tr>
<tr><td>≥2.5</td><td>0 to 0.5</td><td>2</td></tr>
<tr><td><2.5</td><td>0 to 0.2f</td><td>2</td></tr>
</table>
Half Rate Mode*3
<table>
<tr><th>Jittered Clock Output Frequency [GHz]</th><th>Setting Range [UIp-p]</th><th>Steps [mUI]</th></tr>
<tr><td>≥2.5</td><td>0 to 0.5</td><td>4</td></tr>
<tr><td><2.5</td><td>0 to 0.2f</td><td>4</td></tr>
</table>
f: Jittered Clock Output Frequency [GHz]
Accuracy: ±4.9 ps ±15% (Jittered Clock Output Frequency: ≥4 GHz)
±7.0 ps ±15% (Jittered Clock Output Frequency: <4 GHz)
PCIe (Data clocked) or PCIe (Common Ref. clock) Filter
Filter: LF (10 kHz to 1.5 MHz) or HF (1.5 MHz to 100 MHz) for PCIe
Amplitude*1:
Full Rate Mode*2
<table>
<tr><th>Jittered Clock Output Frequency [GHz]</th><th>LF and HF Setting Range [ps rms]</th><th>Steps [ps rms]</th></tr>
<tr><td>>4</td><td>0 to 8.8</td><td>0.1</td></tr>
</table>
Half Rate Mode*2
<table>
<tr><th>Jittered Clock Output Frequency [GHz]</th><th>LF and HF Setting Range [ps rms]</th><th>Steps [ps rms]</th></tr>
<tr><td>>4</td><td>0 to 8.8</td><td>0.2</td></tr>
</table>
LF Amplitude ≥ HF Amplitude
Accuracy: ±0.6 ps ±10%
On/Off Function: Supported
</td></tr>
<tr><td>Bounded Uncorrelated Jitter (BUJ)</td><td>
PRBS Pattern Length: $2^n - 1$ (n = 7, 9, 11, 15, 23, or 31)
BUJ Rate: 0.1 Gbit/s to 3.2 Gbit/s, Steps: 1 kbit/s
4.9 Gbit/s to 6.25 Gbit/s, Steps: 1 kbit/s (Jittered Clock Output Frequency: >4 GHz)
9.8 Gbit/s to 12.5 Gbit/s, Steps: 1 kbit/s (Jittered Clock Output Frequency: >4 GHz)
Filter Type (LPF 3 dB Bandwidth): 50, 100, 200, 300, 500 MHz, Through (Jittered Clock Output Frequency: >4 GHz)
50, 100, 200, 300 MHz, Through (Jittered Clock Output Frequency: ≤4 GHz)
Amplitude*1:
Full Rate Mode*2
<table>
<tr><th>Jittered Clock Output Frequency [GHz]</th><th>Setting Range [UIp-p]</th><th>Steps [mUI]</th></tr>
<tr><td>≥2.5</td><td>0 to 0.5</td><td>2</td></tr>
<tr><td><2.5</td><td>0 to 0.2f</td><td>2</td></tr>
</table>
Half Rate Mode*2
<table>
<tr><th>Jittered Clock Output Frequency [GHz]</th><th>Setting Range [UIp-p]</th><th>Steps [mUI]</th></tr>
<tr><td>≥2.5</td><td>0 to 0.5</td><td>4</td></tr>
<tr><td><2.5</td><td>0 to 0.2f</td><td>4</td></tr>
</table>
f: Jittered Clock Output Frequency [GHz]
Accuracy: ±4.9 ps ±15% (Jittered Clock Output Frequency: ≥4 GHz)
±7.0 ps ±15% (Jittered Clock Output Frequency: <4 GHz)
PRBS Pattern Length: $2^n - 1$ (n = 7, 9)
BUJ Rate: 6, 5.5, 4.9 Gbit/s, LPF 500 MHz
BUJ Rate: 3.2 Gbit/s, 3 Gbit/s, LPF 300 MHz
BUJ Rate: 3.2 Gbit/s, 2 Gbit/s, LPF 200 MHz
BUJ Rate: 2 Gbit/s, 1.1 Gbit/s, LPF 100 MHz
On/Off Function: Supported
</td></tr>
<tr><td>External Jitter</td><td>
Bandwidth: 10 kHz to 1 GHz
Accuracy*3: 0.5 UI ±10% (2 Vp-p)
Linearity*3: ±6 ps ±10%
On/Off Function: Supported
</td></tr>
</table>

∗1: The maximum jitter amplitude is limited according to the jitter tolerance of PPG or ED modules. Refer to the jitter tolerance specification of PPG/ED modules.
∗2: Full Rate Mode: MU181020A/B PPG or MU182020A/21A MUX as a Full Rate
Half Rate Mode: MU182020A/21A MUX as a Half Rate
∗3: Jittered Clock Output Frequency: Specified as 5 GHz, Modulation Frequency: 0.5 GHz, Sinusoidal Jitter

● MU181800A 12.5 GHz Clock Distributor

Frequency Range	0.1 GHz to 12.5 GHz
Clock Input	Level: 0.4 Vp-p to 2.0 Vp-p Waveform: Square wave (<0.5 GHz), Square wave or Sine wave (≥0.5 GHz) Connector: SMA(f.), Termination: 50Ω/GND
Clock Output	4ch Single-end Level: 0.4 Vp-p (Min.), 1.0 Vp-p (Max.) Duty: 50±10% (50% Clock Input Duty) Channel Skew: ≤10 ps (12.5 GHz) Connector: SMA(f.), Termination: 50Ω/GND

● MU181800B 14 GHz Clock Distributor

Frequency Range	0.1 GHz to 14 GHz
Clock Input	Level: 0.4 Vp-p to 2.0 Vp-p Waveform: Square wave (<0.5 GHz), Square wave or Sine wave (≥0.5 GHz) Connector: SMA(f.), Termination: 50Ω/GND
Clock Output	5ch Single-end Level: 0.4 Vp-p (Min.), 1.0 Vp-p (Max.) Duty: 50±10% (50% Clock Input Duty) Channel Skew: ≤10 ps (14 GHz) Connector: SMA(f.), Termination: 50Ω/GND

● MU181020A 12.5 Gbit/s PPG

	MU181020A-001 9.8 Gbit/s to 12.5 Gbit/s	MU181020A-002 0.1 Gbit/s to 12.5 Gbit/s
Bit Rate	9.8 Gbit/s to 12.5 Gbit/s 1/2 Mode: 4.9 Gbit/s to 6.25 Gbit/s 1/4 Mode: 2.45 Gbit/s to 3.125 Gbit/s 1/8 Mode: 1.225 Gbit/s to 1.5625 Gbit/s	0.1 Gbit/s to 12.5 Gbit/s
Built-in Clock	9.8 GHz to 12.5 GHz 1/2 Mode: 4.9 GHz to 6.25 GHz 1/4 Mode: 2.45 GHz to 3.125 GHz 1/8 Mode: 1.225 GHz to 1.5625 GHz Setting Steps: 1 kHz/1 MHz	No built-in clock source
External Clock Input	Frequency: 9.8 GHz to 12.5 GHz or (9.8 GHz to 12.5 GHz)/64 Level: 0.4 Vp-p (Min.), 2.0 Vp-p (Max.) (–4 to +10 dBm) Waveform: Square wave (<0.5 GHz) Square wave or Sine wave (≥0.5 GHz) Duty: 50% Connector: SMA(f.), Termination: 50Ω/AC Coupling	Frequency: 0.1 GHz to 12.5 GHz Level: 0.4 Vp-p (Min.), 2.0 Vp-p (Max.) (–4 to +10 dBm) Waveform: Square wave (<0.5 GHz) Square wave or Sine wave (≥0.5 GHz) Duty: 50% Connector: SMA(f.), Termination: 50Ω/AC Coupling
Generation Pattern	PRBS Steps: 2^n–1 (n = 7, 9, 10, 11, 15, 20, 23, 31) Mark Ratio: 1/2, 1/4, 1/8, 0/8; $\overline{1/2}$, 3/4, 7/8, 8/8 supported at reverse logic AND Bit Shift: 1 bit, 3 bits (Prohibited at 1/2, $\overline{1/2}$, 0/8, 8/8 mark ratio) Zero Substitution Pattern with continuous 0s appended to M-sequence signal+1 bit Pattern: 2^n or 2^n–1 (n = 7, 9, 10, 11, 15, 20, 23) 0 continuous substitution count: 1 to (pattern length–1) bits Other: 0 at next bit after 0 substitution changed to 1 Data Data Length: 2 to 134217728 bits/ch, Steps: 1 bit Alternate Data Length: 128 to 67108864 bits/ch (independent bits for A/B) Steps: 128 bits Loop Count: 511 times (A/B set independently) A/B Switching: Auto-switching by A/B loop times setting (Internal) Controlled by external signal (External) Editing: Pattern editing for A/B independently Mixed Pattern Pattern: PRBS, Data-1 to Data-511 Data+PRBS Length: 768 to 2^{31}+134217728, Steps: 128 bits Data Length: 512 to 134217728 bits Sequence Pattern Block Count: 1 to 128 Block Length: 8192 to 1048576 bits, Steps: 128 bits Loop Count: 1 to 1024 times, Repeat Block Transition Conditions: A pattern match, B pattern match, Manual, Loop Time complete, External trigger (rising edge) Next Destination: Specified Block No. or Stop	
Error Insertion	Error Event: Repeat, Single Error rate: #E–n (# = 1 to 9, n = 2 to 12) Timing: Internal/External	
Auxiliary Input	ALTN Trigger/Sequence Trigger/Error Injection/Burst Enable (Switchable) Frequency: ≥64 bits width Level: H: 0 V, L:–1 V Connector: SMA(f.), Termination: 50Ω/GND	
Auxiliary Output	1/1 Mode: 1/n clock (2, 4, 8, 9...., 511) 1/2 Mode: 1/n clock (1, 2, 4, 8, 9...., 255) 1/4 Mode: 1/n clock (1, 2, 4, 8, 9...., 127) 1/8 Mode: 1/n clock (1, 2, 4, 8, 9...., 63) Pattern Sync, Burst Trigger Level: H: 0 V, L: –1 V Connector: SMA(f.), Termination: 50Ω/GND	1/n Clock (n = 2, 4, 8, 9, 10, 11…….510, 511) Pattern Sync, Burst Trigger Level: H: 0 V, L: –1 V Connector: SMA(f.), Termination: 50Ω/GND
Gating Output	Burst Output Signal at Burst, Timing Signal at Repeat 1ch Output Level: H: 0 V, L: –1 V Connector: SMA(f.), Termination: 50Ω/GND	
MU181020A-030 Variable Data Delay [MU181020A-002]	—	Independent Mode Phase Setting Range: –1 UI to +1 UI, Steps: 1 mUI, Unit: UI/ps CH Synchronization or Combination Mode Phase Setting Range: –64 UI to +64 UI, Steps: 1 mUI, Unit: UI/ps

● MU181020A 12.5 Gbit/s PPG Amplitude Option

		No Option	MU181020A-010	MU181020A-011	MU181020A-012	MU181020A-013
Number of Output		2 (Data/$\overline{\text{Data}}$)				
Data Output	Amplitude	—	0.05 Vp-p to 0.8 Vp-p Steps: 2 mV Setting Accuracy: ±50 mV±17%	0.25 Vp-p to 2.5 Vp-p Steps: 2 mV Setting Accuracy: ±50 mV±17%	0.05 Vp-p to 2.0 Vp-p Steps: 2 mV Setting Accuracy: ±50 mV±17%	0.5 Vp-p to 3.5 Vp-p Steps: 2 mV Setting Accuracy: ±50 mV±17%
	Offset	—	–2.0 Voh to +3.3 Voh Steps: 1 mV			
	Current Limiting	—	Sourcing 50 mA, Sinking 80 mA			
	Level	MU181020A-001 H: 0 V, L: –0.5 V MU181020A-002 H: 0 V, L: –1.0 V	—	—	—	—
	Fixed Interface	—	NECL, SCFL, NCML, PCML, LVPECL (+3.3 V), LVDS			NECL, SCFL, NCML, PCML, LVPECL
	Crosspoint	50±15%	30 to 70% Steps: 1%		20 to 80% Steps: 1%	20 to 90% Steps: 0.1%
	Tr/Tf	MU181020A-001 30 ps (typ.) (20 to 80%) (≥5 Gbit/s) MU181020A-002 35 ps (typ.) (20 to 80%) (≥5 Gbit/s)	28 ps (typ.) (20 to 80%) (≥5 Gbit/s)		20 ps (typ.) (20 to 80%) (10 Gbit/s, 12.5 Gbit/s, Amplitude: 2 Vp-p)	25 ps (typ.) (20 to 80%) (10 Gbit/s, Amplitude: ≥1 Vp-p)
	Total Jitter	MU181020A-001 15 ps (typ.) MU181020A-002 10 ps (typ.)	MU181020A-001 15 ps p-p (typ.) MU181020A-002 10 ps p-p (typ.)		MU181020A-001 15 ps p-p (typ.) MU181020A-002 8 ps p-p (typ.)	MU181020A-001/002 8 ps p-p (typ.)
	Distortion (0-peak)	—	±14% (typ.)	±25 mV ±6% (typ.)		±25 mV ±10% (typ.)
	Connector	SMA(f.)		K(f.)		
	Termination	GND/50Ω	AC, DC DC: GND, –2 V, +1.3 V, +3.3 V, Open (LVDS)/50Ω			AC, DC DC: GND, –2 V, +1.3 V, +3.3 V/50Ω
	On/Off Function	Always On	Supported			

● MU181020A 12.5 Gbit/s PPG Clock Option

		No Option	MU181020A-021 Differential Clock Output
Clock Output	Number of Output	1 (Clock)	2 (Clock/$\overline{\text{Clock}}$)
	Amplitude	0.25 Vp-p (Min.), 0.9 Vp-p (Max.) (AC)	0.1 Vp-p to 2.0 Vp-p, Steps: 2 mV
	Duty	50±15%	25 to 75, Steps: 1
	Offset	—	–2.0 Voh to +3.3 Voh, Steps: 1 mV
	Current Limiting	—	Sourcing: 50 mA, Sinking: 80 mA
	Fixed Interface	—	NECL, SCFL, NCML, PCML, LVPECL (+3.3 V), LVDS
	Tr/Tf	30 ps (typ.) (20 to 80%)	24 ps (typ.) (20 to 80%)
	Total Jitter	MU181020A-001: 2 ps (typ.) (RMS) MU181020A-002: 1 ps (typ.) (RMS)	MU181020A-001: 2 ps (typ.) (RMS) MU181020A-002: 1 ps (typ.) (RMS)
	Connector	SMA(f.)	K(f.)
	Termination	GND/50Ω	AC, DC DC: GND, –2 V, +1.3 V, +3.3 V, Open (LVDS)/50Ω
	On/Off Function	Always On	Supported

● MU181020B 14 Gbit/s PPG

	MU181020B-002 0.1 Gbit/s to 14 Gbit/s
Bit Rate	0.1 Gbit/s to 14 Gbit/s 0.1 Gbit/s to 14.05 Gbit/s [MU181020B-003]
External Clock Input	Frequency: 0.1 GHz to 14 GHz 0.1 GHz to 14.05 GHz [MU181020B-003] Level: 0.4 Vp-p (Min.), 1.5 Vp-p (Max.) (–4 to +7.5 dBm) Waveform: Square wave (<0.5 GHz), Square wave or Sine wave (≥0.5 GHz) Duty: 50% Connector: SMA(f.), Termination: 50Ω/AC Coupling
Generation Pattern	PRBS Steps: 2^n–1 (n = 7, 9, 10, 11, 15, 20, 23, 31) Mark Ratio: 1/2, 1/4, 1/8, 0/8; $\overline{1/2}$, 3/4, 7/8, 8/8 supported at reverse logic AND Bit Shift: 1 bit, 3 bits (Prohibited at 1/2, $\overline{1/2}$, 0/8, 8/8 mark ratio) Zero Substitution Pattern with continuous 0s appended to M-sequence signal+1 bit Pattern: 2^n or 2^n–1 (n = 7, 9, 10, 11, 15, 20, 23) 0 continuous substitution count: 1 to (pattern length–1) bits Other: 0 at next bit after 0 substitution changed to 1 Data Data Length: 2 to 134217728 bits/ch, Steps: 1 bit Alternate Data Length: 128 to 67108864 bits/ch (independent bits for A/B), Steps: 128 bits Loop Count: 511 times (A/B set independently) A/B Switching: Auto-switching by A/B loop times setting (Internal) Controlled by external signal (External) Editing: Pattern editing for A/B independently Mixed Pattern Pattern: PRBS, Data-1 to Data-511 Data+PRBS Length: 768 to 2^{31}+134217728, Steps: 128 bits Data Length: 512 to 134217728 bits Sequence Pattern Block Count: 1 to 128 Block Length: 16384 to 1048576 bits, Steps: 128 bits Loop Count: 1 to 1024 times, Repeat Block Transition Conditions: A pattern match, B pattern match, Manual, Loop Time complete, External trigger (rising edge) Next Destination: Specified Block No. or Stop
Error Insertion	Error Event: Repeat, Single Error rate: #E–n (# = 1 to 9, n = 2 to 12) Timing: Internal/External
Auxiliary Input	ALTN Trigger/Sequence Trigger/Error Injection/Burst Enable (Switchable) Frequency: ≥64 bit width Level: H: 0 V, L: –1 V Connector: SMA(f.), Termination: 50Ω/GND
Auxiliary Output	1/n Clock (n = 2, 4, 8, 9, 10, 11……., 510, 511) Pattern Sync, Burst Trigger Level: H: 0 V, L: –1 V Connector: SMA(f.), Termination: 50Ω/GND
Gating Output	Burst Output Signal at Burst, Timing Signal at Repeat 1ch Output Level: H: 0 V, L: –1 V Connector: SMA(f.), Termination: 50Ω/GND
Variable Data Delay [MU181020B-030/130]	Independent Mode Phase Setting Range: –1 UI to +1 UI, Steps: 1 mUI, Unit: UI/ps CH Synchronization or Combination Mode Phase Setting Range: –64 UI to +64 UI, Steps: 1 mUI, Unit: UI/ps
Operation Temperatures	15° to 35°C

● MU181020B 14 Gbit/s PPG Amplitude Option

		No Option	MU181020B-011	MU181020B-012	MU181020B-013
Number of Output		2 (Data/$\overline{\text{Data}}$)			
Data Output	Amplitude	—	0.25 Vp-p to 2.5 Vp-p Steps: 2 mV Setting Accuracy: ±50 mV±17%	0.05 Vp-p to 2.0 Vp-p Steps: 2 mV Setting Accuracy: ±50 mV±17%	0.5 Vp-p to 3.5 Vp-p Steps: 2 mV Setting Accuracy: ±50 mV±17%
	Offset	—	–2.0 Voh to +3.3 Voh Steps: 1 mV		
	Current Limiting	—	Sourcing 50 mA, Sinking 80 mA		
	Level	H: 0 V, L: –1.0 V	—	—	—
	Fixed Interface	—	NECL, SCFL, NCML, PCML, LVPECL (+3.3 V), LVDS		NECL, SCFL, NCML, PCML, LVPECL
	Crosspoint	50±15%	30 to 70%, Steps: 1%	20 to 80%, Steps: 1%	20 to 90%, Steps: 0.1%
	Tr/Tf	35 ps (typ.) (20 to 80%) (≥5 Gbit/s)	28 ps (typ.) (20 to 80%) (≥5 Gbit/s)	20 ps (typ.) (20 to 80%) (10, 12.5, 14 Gbit/s, Amplitude: 2 Vp-p)	25 ps (typ.) (20 to 80%) (10 Gbit/s, Amplitude: ≥1 Vp-p)
	Total Jitter	10 ps (typ.)	10 ps p-p (typ.)	8 ps p-p (typ.)	
	Distortion (0-peak)	—	±25 mV ±6% (typ.)		±25 mV ±10% (typ.)
	Connector	SMA(f.)	K(f.)		
	Termination	GND/50Ω	AC, DC DC: GND, –2 V, +1.3 V, +3.3 V, Open (LVDS)/50Ω		AC, DC DC: GND, –2 V, +1.3 V, +3.3 V/50Ω
	On/Off Function	Always On	Supported		

● MU181020B 14 Gbit/s PPG Clock Option

		No Option	MU181020B-021 Differential Clock Output
Clock Output	Number of Output	1 (Clock)	2 (Clock/$\overline{\text{Clock}}$)
	Amplitude	0.25 Vp-p (Min.), 0.9 Vp-p (Max.) (AC)	0.1 Vp-p to 2.0 Vp-p, Steps: 2 mV
	Duty	50±15%	25 to 75, Steps: 1
	Offset	—	–2.0 Voh to +3.3 Voh, Steps: 1 mV
	Current Limiting	—	Sourcing: 50 mA, Sinking: 80 mA
	Fixed Interface	—	NECL, SCFL, NCML, PCML, LVPECL (+3.3 V), LVDS
	Tr/Tf	30 ps (typ.) (20 to 80%)	24 ps (typ.) (20 to 80%)
	Total Jitter	1 ps (typ.) (RMS)	1 ps (typ.) (RMS)
	Connector	SMA(f.)	K(f.)
	Termination	GND/50Ω	AC, DC DC: GND, –2 V, +1.3 V, +3.3 V, Open (LVDS)/50Ω
	On/Off Function	Always On	Supported

● MU181040A 12.5 Gbit/s ED

		MU181040A-001 9.8 Gbit/s to 12.5 Gbit/s	MU181040A-002 0.1 Gbit/s to 12.5 Gbit/s	
Bit Rate		9.8 Gbit/s to 12.5 Gbit/s	0.1 Gbit/s to 12.5 Gbit/s	
Reception Pattern		PRBS Steps: 2^n–1 (n = 7, 9, 10, 11, 15, 20, 23, 31) Mark Ratio: 1/2, 1/4, 1/8, 0/8; $\overline{1/2}$, 3/4, 7/8, 8/8 supported at reverse logic AND Bit Shift: 1 bit, 3 bits (Prohibited at 1/2, $\overline{1/2}$, 0/8, 8/8 mark ratio) Zero Substitution Pattern with continuous 0s appended to M-sequence signal+1 bit Pattern: 2^n or 2^n–1 (n = 7, 9, 10, 11, 15, 20, 23) 0 continuous substitution count: 1 to (pattern length–1) bits Other: 0 at next bit after 0 substitution changed to 1 Data Data Length: 2 to 134217728 bits/ch, Steps: 1 bit Mixed Pattern Pattern: PRBS, Data-1 to Data-511 Data+PRBS Length: 768 to 2^{31}+134217728, Steps: 128 bits Data Length: 512 to 134217728 bits Sequence Pattern Block Count: 1 to 128		
Detection Item		Total Error, Insertion Error, Omission Error, Transition Error, Non-Transition Error		
Display Item		Bit Error Rate, Bit Error Count, Input Signal Frequency		
Input Signal Synchronization		Auto Sync. On/Off		
Error Analysis		Input Signal Capture (128 Mbits), Eye Margin, Eye Diagram, Q Measurement, Bathtub, ISI Analysis		
Burst Signal Measurement		Burst Trigger: Internal/External Input		
Option Number		No Option		MU181040A-020*
Clock Recovery	Frequency Range	9.8 GHz to 12.5 GHz	—	0.1 GHz 0.125 GHz to 0.2 GHz 0.25 GHz to 0.4 GHz 0.5 GHz to 0.8 GHz 1 GHz to 1.6 GHz 2 GHz to 3.2 GHz 4.25 GHz 4.9 GHz to 6.25 GHz 9.8 GHz to 12.5 GHz
	Recovered Clock Output	—	—	POS/NEG reversible [without MU181040A-030] Amplitude: 0.55 ±0.15 Vp-p Connector: SMA(f.)
Clock Input	Frequency Range	—	0.1 GHz to 12.5 GHz	
	Clock Source Waveform	—	Internal/External [MU181040A-020] Waveform: Square wave (<0.5 GHz) Square wave or Sine wave (≥0.5 GHz) Duty: 50%	
	Number of Input	—	1	
	Level	—	0.25 Vp-p (Min.), 2.0 Vp-p (Max.)	
	Connector	—	SMA(f.)	
	Termination	—	GND/50Ω, Variable/50Ω, Differential/100Ω NECL, PCML (+3.3 V), LVPECL (+3.3 V), GND Variable: –2.5 V to +3.5 V, Steps: 10 mV	
Data Input	Number of Input	2 (Data, $\overline{\text{Data}}$)		
	Signal Format	NRZ		
	Amplitude	0.1 Vp-p (Min.), 0.9 Vp-p (Max.)	0.1 Vp-p (Min.), 2.0 Vp-p (Max.)	
	Threshold	–0.35 V to +0.35 V, Steps: 1 mV	–3.5 V to +3.3 V, Steps: 1 mV	
	Sensitivity	<50 mVp-p (12.5 Gbit/s, PRBS2^{31}–1)	10 mVp-p (typ.) (12.5 Gbit/s, PRBS2^{31}–1)	
	Phase Margin	—	60 ps p-p (typ.) (12.5 Gbit/s, PRBS2^{31}–1)	
	Connector	SMA(f.)	K(f.)	
	Termination	50Ω/AC Coupling	GND/50Ω, Variable/50Ω, Differential/100Ω NECL, PCML (+3.3 V), LVPECL (+3.3 V), GND Variable: –2.5 V to +3.5 V, Steps: 10 mV	
Auxiliary Input		Sequence Trigger/Capture Trigger/Burst Enable (switchable) Frequency: ≥64 bit width Level: H: 0 V, L: –1 V Connector: SMA(f.), Termination: 50Ω/GND		
Auxiliary Output		1/16 Clock, 1/32 Clock, 1/64 Clock, Pattern Sync, Error, Sync Gain Level: H: 0 V, L: –1 V	1/N Clock (N = 8 to 511), Steps: 1, Pattern Sync, Error, Sync Gain Level: H: 0 V, L: –1 V	
Data Monitor Output	Number of Output	—	2 (Data, $\overline{\text{Data}}$)	
	Insertion Loss	—	–6 dB +1/–2 dB	
	Connector	—	SMA(f.)	
	Termination	—	50Ω/AC Coupling	
MU181040A-030 Variable Clock Delay [MU181040A-002]		—	Phase Setting Range: –1 UI to +1 UI, Steps: 1 mUI, Unit: UI/ps	

*: We recommend adding the option of MU181040A/B-030/130 Variable Clock Delay when using MU181040A/B-020/120 Clock Recovery.

● MU181040B 14 Gbit/s ED

		MU181040B-002 0.1 Gbit/s to 14 Gbit/s	
Bit Rate		0.1 Gbit/s to 14 Gbit/s 0.1 Gbit/s to 14.05 Gbit/s [MU181040B-003]	
Reception Pattern		PRBS Steps: 2^n–1 (n = 7, 9, 10, 11, 15, 20, 23, 31) Mark Ratio: 1/2, 1/4, 1/8, 0/8; $\overline{1/2}$, 3/4, 7/8, 8/8 supported at reverse logic AND Bit Shift: 1 bit, 3 bits (Prohibited at 1/2, $\overline{1/2}$, 0/8, 8/8 mark ratio) Zero Substitution Pattern with continuous 0s appended to M-sequence signal +1 bit Pattern: 2^n or 2^n–1 (n = 7, 9, 10, 11, 15, 20, 23) 0 continuous substitution count: 1 to (pattern length–1) bits Other: 0 at next bit after 0 substitution changed to 1 Data Data Length: 2 to 134217728 bits/ch, Steps: 1 bit Mixed Pattern Pattern: PRBS, Data-1 to Data-511 Data+PRBS Length: 768 to 2^{31}+134217728, Steps: 128 bits Data Length: 512 to 134217728 bits Sequence Pattern Block Count: 1 to 128	
Detection Item		Total Error, Insertion Error, Omission Error, Transition Error, Non-Transition Error	
Display Item		Bit Error Rate, Bit Error Count, Input Signal Frequency	
Input Signal Synchronization		Auto Sync.: On/Off	
Error Analysis		Input Signal Capture (128 Mbits), Eye Margin, Eye Diagram, Q Measurement, Bathtub, ISI Analysis	
Burst Signal Measurement		Burst Trigger: Internal/External Input	
Option Number		No Option	MU181040B-020*
Clock Recovery	Frequency Range	—	0.1 GHz, 0.125 GHz to 0.2 GHz, 0.25 GHz to 0.4 GHz, 0.5 GHz to 0.8 GHz, 1 GHz to 1.6 GHz, 2 GHz to 3.2 GHz, 4.25 GHz, 4.9 GHz to 6.25 GHz, 9.8 GHz to 12.5 GHz
	Recovered Clock Output	—	POS/NEG reversible [without MU181040B-030] Amplitude: 0.55 ±0.15 Vp-p Connector: SMA(f.)
Clock Input		Operating Frequency Range: 0.1 GHz to 14 GHz 0.1 GHz to 14.05 GHz [MU181040B-003] Clock Source Waveform: Internal/External [MU181040B-020] Waveform: Square wave (<0.5 GHz), Square wave or Sine wave (≥0.5 GHz) Duty 50% Number of Input: 1 Level: 0.25 Vp-p (Min.), 1.5 Vp-p (Max.) Connector: SMA(f.) Termination: GND/50Ω, Variable/50Ω, Differential/100Ω NECL, PCML (+3.3 V), LVPECL (+3.3 V), GND Variable: –2.5 V to +3.5 V, Steps: 10 mV	
Data Input		Number of Input: 2 (Data, $\overline{\text{Data}}$) Signal Format: NRZ Amplitude: 0.1 Vp-p (Min.), 2.0 Vp-p (Max.) Threshold: –3.5 V to +3.3 V, Steps: 1 mV Input Sensitivity: 20 mVp-p (typ.) (14 Gbit/s PRBS 2^{31}–1) Phase Margin: 50 ps p-p (typ.) (14 Gbit/s PRBS 2^{31}–1) Connector: K(f.) Termination: GND/50Ω, Variable/50Ω, Differential/100Ω NECL, PCML (+3.3 V), LVPECL (+3.3 V), GND Variable: –2.5 V to +3.5 V, Steps: 10 mV	
Auxiliary Input		Sequence Trigger/Capture Trigger/Burst Enable (switchable) Frequency: ≥64 bit width Level: H: 0 V, L: –1 V Connector: SMA(f.), Termination: 50Ω/GND	
Auxiliary Output		1/N Clock (N = 8 to 511), Steps: 1 Pattern Sync, Error, Sync Gain Level: H: 0 V, L: –1 V	
Data Monitor Output		Number of Output: 2 (Data, $\overline{\text{Data}}$) Insertion Loss: –6 dB +1/–2.5 dB Connector: SMA(f.), Termination: 50Ω/AC Coupling	
Variable Clock Delay [MU181040B-030/130]		Phase Setting Range: –1 UI to +1 UI, Steps: 1 mUI, Unit: UI/ps	
Operation Temperatures		15° to 35°C	

*: We recommend adding the option of MU181040A/B-030/130 Variable Clock Delay when using MU181040A/B-020/120 Clock Recovery.

● MU182020A 25 Gbit/s 1ch MUX

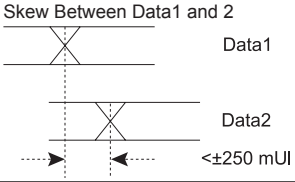
Bit Rate	8 Gbit/s to 25 Gbit/s 8 Gbit/s to 28 Gbit/s [MU182020A-001] 8 Gbit/s to 28.1 Gbit/s [MU182020A-001, 003]
External Clock Input	Frequency Range: 4.0 GHz to 12.5 GHz 4.0 GHz to 14.0 GHz [MU182020A-001] 4.0 GHz to 14.05 GHz [MU182020A-001, 003] 4.0 GHz to 12.5 GHz, 8.0 GHz to 25.0 GHz [MU182020A-002] 4.0 GHz to 14.0 GHz, 8.0 GHz to 28.0 GHz [MU182020A-001, 002] 4.0 GHz to 14.05 GHz, 8.0 GHz to 28.1 GHz [MU182020A-001, 002, 003] Amplitude: 0.3 Vp-p to 1.0 Vp-p Connector: SMA(f.) K(f.) [MU182020A-002]
Data Output*	Number of Output: 2 (Data, xData) Amplitude: 0.25 Vp-p to 1.75 Vp-p, Steps: 2 mV [MU182020A-010] 0.5 Vp-p to 2.5 Vp-p, Steps: 2 mV [MU182020A-011] 0.5 Vp-p to 3.5 Vp-p, Steps: 2 mV [MU182020A-013] Amplitude Setting Accuracy: ±50 mV ±17% (Cross point: 50% or 30 to 80%, 25 Gbit/s) Offset: –2.0 Voh to +3.3 Voh, Steps: 1 mV Cross Point Adjust: 20 to 80%, Steps: 0.1% (25 Gbit/s) Tr/Tf: 12 ps (typ.) (20 to 80%) Total Jitter: 8 ps p-p (typ.) Distortion (0-peak): ±25 mV ±10% (typ.) (25 Gbit/s) Connector: K(f.) On/Off Function: Supported
Clock Output	Frequency: Output clock frequency is same of input clock frequency Number of Output: 1 (Clock) Amplitude: 0.3 Vp-p (Min.), 1.0 Vp-p (Max.) (Fixed) 0.7 Vp-p (Min.), 1.0 Vp-p (Max.) (Fixed) [MU182020A-002] 0.5 Vp-p to 2.0 Vp-p, Steps: 2 mV [MU182020A-021] Offset: –2.0 Voh to +3.3 Voh, Steps: 1 mV [MU182020A-021] Duty: –25 to +25, Steps: 1 [MU182020A-021] Connector: SMA(f.) K(f.) [MU182020A-002 or 021] On/Off Function: Supported [MU182020A-002 or 021]
1/2 Data Input	Number of Input: 2 (1/2 Data Input A, 1/2 Data Input B) Amplitude: 0 V, –1.0 V Connector: SMA(f.)
1/2 Clock Input	Number of Input: 1 Amplitude: 0.25 Vp-p to 1.0 Vp-p Connector: SMA(f.)
1/2 Clock Output	Number of Output: 2 Amplitude: 0.4 Vp-p (Min.), 1.2 Vp-p (Max.) Connector: SMA(f.)
Data Output Delay [MU182020A-030 or 031]	Phase Variable Range: –2000 mUI to +2000 mUI, Steps: 2 mUI Phase Setting Error: 50 mUIp-p (typ.)
Operation Temperatures	15° to 35°C

∗: The above specifications were measured with the oscilloscope, intrinsic jitter should be less than 200 fs (rms), and more than 70 GHz bandwidth.

● MU182040A 25 Gbit/s 1ch DEMUX

Bit Rate	8 Gbit/s to 25 Gbit/s 8 Gbit/s to 28 Gbit/s [MU182040A-001] 8 Gbit/s to 28.1 Gbit/s [MU182040A-001, 003]
External Clock Input	Frequency Range: 4.0 GHz to 12.5 GHz 4.0 GHz to 14.0 GHz [MU182040A-001] 4.0 GHz to 14.05 GHz [MU182040A-001, 003] 4.0 GHz to 12.5 GHz, 8.0 GHz to 25.0 GHz [MU182040A-002] 4.0 GHz to 14.0 GHz, 8.0 GHz to 28.0 GHz [MU182040A-001, 002] 4.0 GHz to 14.05 GHz, 8.0 GHz to 28.1 GHz [MU182040A-001, 002, 003] Amplitude: 0.3 Vp-p to 1.0 Vp-p Connector: SMA(f.) K(f.) [MU182040A-002]
Data Input	Signal Format: NRZ Number of Input: 2 (Data, xData) Single-ended/Differential selectable Amplitude: 0.25 Vp-p to 2.0 Vp-p Threshold Voltage: –3.5 V to +3.3 V, Steps: 1 mV Sensitivity: 50 mVp-p (typ.) (25 Gbit/s, PRBS31) Phase Margin: 28 ps (typ.) (25 Gbit/s, PRBS31) Connector: K(f.) Termination: 50Ω/GND, 50Ω/Variable (–2.5 V to +3.5 V)
1/2 Data Output	Number of Output: 2 (1/2 DataA, 1/2 DataB) Amplitude: 0 V, –0.4 V Connector: SMA(f.)
1/2 Clock Output	Number of Output: 2 Amplitude: 0.4 Vp-p (Min.), 1.2 Vp-p (Max.) Connector: SMA(f.)
Variable Clock Delay [MU182040A-030 or 031]	Phase Variable Range: –2000 mUI to +2000 mUI, Steps: 2 mUI Phase Setting Error: 50 mUIp-p (typ.)
Auto Search Function	Supported
Operation Temperatures	15° to 35°C

● MU182021A 25 Gbit/s 2ch MUX

Bit Rate	8 Gbit/s to 25 Gbit/s 8 Gbit/s to 28 Gbit/s [MU182021A-001] 8 Gbit/s to 28.1 Gbit/s [MU182021A-001, 003]
External Clock Input	Frequency Range: 4.0 GHz to 12.5 GHz 4.0 GHz to 14.0 GHz [MU182021A-001] 4.0 GHz to 14.05 GHz [MU182021A-001, 003] 4.0 GHz to 12.5 GHz, 8.0 GHz to 25.0 GHz [MU182021A-002] 4.0 GHz to 14.0 GHz, 8.0 GHz to 28.0 GHz [MU182021A-001, 002] 4.0 GHz to 14.05 GHz, 8.0 GHz to 28.1 GHz [MU182021A-001, 002, 003] Amplitude: 0.3 Vp-p to 1.0 Vp-p Connector: SMA(f.) K(f.) [MU182021A-002]
Data Output*	Number of Output: 4 (Data1, xData1, Data2, xData2) Amplitude: 0.25 Vp-p to 1.75 Vp-p, Steps: 2 mV [MU182021A-010] 0.5 Vp-p to 2.5 Vp-p, Steps: 2 mV [MU182021A-011] 0.5 Vp-p to 3.5 Vp-p, Steps: 2 mV [MU182021A-013] Amplitude Setting Accuracy: ±50 mV ±17% (Cross point: 50% or 30 to 80%, 25 Gbit/s) Offset: –2.0 Voh to +3.3 Voh, Steps: 1 mV Cross Point Adjust: 20 to 80%, Steps: 0.1% (25 Gbit/s) Tr/Tf: 12 ps (typ.) (20 to 80%) Total Jitter: 8 ps p-p (typ.) Distortion (0-peak): ±25 mV ±10% (typ.) (25 Gbit/s) Connector: K(f.) On/Off Function: Supported
Clock Output	Frequency: Output clock frequency is same of input clock frequency Number of Output: 1 (Clock) 2 (Clock/xClock) [MU182021A-021] Amplitude: 0.3 Vp-p (Min.), 1.0 Vp-p (Max.) (Fixed) 0.7 Vp-p (Min.), 1.0 Vp-p (Max.) (Fixed) [MU182021A-002] 0.5 Vp-p to 2.0 Vp-p, Steps: 2 mV [MU182021A-021] Offset: –2.0 to +3.3 Voh, Steps: 1 mV [MU182021A-021] Duty: –25 to +25, Steps: 1 [MU182021A-021] Connector: SMA(f.) K(f.) [MU182021A-002 or 021] On/Off Function: Supported [MU182021A-002 or 021]
1/2 Data Input	Number of Input: 4 (1/2 Data1A, 1/2 Data1B, 1/2 Data2A, 1/2 Data2B) Amplitude: 0 V, –1.0 V Connector: SMA(f.)
1/2 Clock Input	Number of Input: 1 Amplitude: 0.25 Vp-p to 1.0 Vp-p Connector: SMA(f.)
1/2 Clock Output	Number of Output: 4 Amplitude: 0.4 Vp-p (Min.), 1.2 Vp-p (Max.) Connector: SMA(f.)
Data Output Delay [MU182021A-030 or 031]	Phase Variable Range: –64000 mUI to +64000 mUI, Steps: 2 mUI Phase Setting Error: 50 mUIp-p (typ.) Skew Between Data1 and 2 
Emphasis Control	Supported [MU182021A-040]
Operation Temperatures	15° to 35°C

*: The above specifications were measured with the oscilloscope, intrinsic jitter should be less than 200 fs (rms), and more than 70 GHz bandwidth.

● MU182041A 25 Gbit/s 2ch DEMUX

Bit Rate	8 Gbit/s to 25 Gbit/s 8 Gbit/s to 28 Gbit/s [MU182041A-001] 8 Gbit/s to 28.1 Gbit/s [MU182041A-001, 003]
External Clock Input	Frequency Range: 4.0 GHz to 12.5 GHz 4.0 GHz to 14.0 GHz [MU182041A-001] 4.0 GHz to 14.05 GHz [MU182041A-001, 003] 4.0 GHz to 12.5 GHz, 8.0 GHz to 25.0 GHz [MU182041A-002] 4.0 GHz to 14.0 GHz, 8.0 GHz to 28.0 GHz [MU182041A-001, 002] 4.0 GHz to 14.05 GHz, 8.0 GHz to 28.1 GHz [MU182041A-001, 002, 003] Amplitude: 0.3 Vp-p to 1.0 Vp-p Connector: SMA(f.) K(f.) [MU182041A-002]
Data Input	Signal Format: NRZ Number of Input: 4 (Data1, xData1, Data2, xData2) Single-ended/Differential selectable Amplitude: 0.25 Vp-p to 2.0 Vp-p Threshold Voltage: –3.5 V to +3.3 V, Steps: 1 mV Sensitivity: 50 mV (typ.) (25 Gbit/s, PRBS31) Phase Margin: 28 ps (typ.) (25 Gbit/s, PRBS31) Connector: K(f.) Termination: 50Ω/GND, 50Ω/Variable (–2.5 V to +3.5 V)
1/2 Data Output	Number of Output: 4 (1/2 Data1A, 1/2 Data1B, 1/2 Data2A, 1/2 Data2B) Amplitude: 0 V, –0.4 V Connector: SMA(f.)
1/2 Clock Output	Number of Output: 4 Amplitude: 0.4 Vp-p (Min.), 1.2 Vp-p (Max.) Connector: SMA(f.)
Variable Clock Delay [MU182041A-030 or 031]	Phase Variable Range: –2000 mUI to +2000 mUI, Steps: 2 mUI Phase Setting Error: 50 mUIp-p (typ.)
Auto Search Function	Supported
Operation Temperatures	15° to 35°C

● MU181600A Optical Transceiver (XFP)

Electrical Input (TD)	Waveform: NRZ Differential Input: 0.2 Vp-p to 0.8 Vp-p Connector: SMA(f.), Termination: 100Ω differential
Electrical Output (RD)	Waveform: NRZ Differential Output: 0.3 Vp-p (Min.), 0.9 Vp-p (Max.) Connector: SMA(f.), Termination: 100Ω differential
1/1 Clock Input	Frequency: 9.5 GHz to 12.5 GHz Level: 0.25 Vp-p to 0.8 Vp-p Connector: SMA(f.), Termination: 50Ω/GND
1/64 Clock Output	Frequency: (1/1 of Clock Input)/64 Level: 0.32 Vp-p (Min.), 0.68 Vp-p (Max.) Tr/Tf: 300 ±100 ps (20 to 80%) Duty: 50±10% Connector: SMA(f.), Termination: 50Ω/GND
1/64 of Clock Input	Frequency: (Operation bit rate)/64, Level: 0.32 Vp-p to 0.8 Vp-p Tr/Tf: 200 ps to 1250 ps (20 to 80%) Duty: 40 to 60% Connector: SMA(f.), Termination: 50Ω/GND
Optical Input/Output	Depends on mounted XFP module
XFP Insertion/Removal Times	100 times (Max.)
Laser Safety[*9]	IEC 60825-1: 2007: CLASS 1 21CFR1040.10[*8]

● MU181601A Optical Transceiver (SFP)

Electrical Input (TD)	Waveform: NRZ Single-ended Input: 0.25 Vp-p to 0.6 Vp-p Connector: SMA(f.), Termination: 50Ω Single-ended
Electrical Output (RD)	Waveform: NRZ Single-ended Output: 0.18 Vp-p (Min.), 1.0 Vp-p (Max.) Connector: SMA(f.), Termination: 50Ω Single-ended
Optical Input/Output	Depends on mounted SFP module
SFP Insertion/Removal Times	100 times (Max.)
Laser Safety[*9]	IEC 60825-1: 2007: CLASS 1 21CFR1040.10[*8]

● MU181620A Stressed Eye Transmitter

Bit Rate		0.1 Gbit/s to 12.5 Gbit/s
Data Input		Frequency: 0.1 Gbit/s to 12.5 Gbit/s Amplitude: 0.8 Vp-p to 1.6 Vp-p Vih Level: 0.0 V (typ.) Signal Format: NRZ (Cross Point: 50±5%) Connector: SMA(f.), Termination: 50Ω/GND
Clock Input		Frequency: 1.0 GHz to 12.5 GHz Amplitude: 0.25 Vp-p to 1.0 Vp-p Connector: SMA(f.), Termination: 50Ω/GND
Noise Input [MU181620A-011/012/013]		Frequency: DC to 3.2 GHz Amplitude: 4.0 Vp-p (Max.) Offset: AC or Vth 0 V Connector: SMA(f.), Termination: 50Ω/GND
Optical Output		
MU181620A-011/013	MU181620A-001/003	1310 nm Reference: MU181620A-001/003/011/013 (MU181620A-003/013: 1310 nm) Output Power (Average): –4.0 dBm (Min.), +4.0 dBm (Max.), +7.0 dBm (Max.) (Non-modulation or input opened) Output Power Stability[*4]: ±0.02 dB Center Wavelength: 1290 nm (Min.), 1330 nm (Max.) Side Mode Suppression Ratio: ≥30 dB Extinction Ratio[*1, 2]: 5.0 to 10.0 dB, Steps: 0.1 dB VECP[*1, 5]: ≤0.5 dB (In the Center 20% Region of the Eye) (Extinction Ratio: 9.0 dB, Use a reference O/E specified by Anritsu) Tr/Tf[*1, 3]: ≤30 ps (20 to 80%) Jitter[*1]: ≤0.2 UIp-p, Compliant with IEEE802.3-2005 Eye Mask[*2, 3]: Compliant with STM64/OC192 (9.95328 Gbit/s), IEEE802.3-2005 Clause 52 (10.3125 Gbit/s, Mask margin≥30%), STM64/OC192 with FEC (10.709 Gbit/s)
		1310 nm Stressed Eye: MU181620A-011/013 (MU181620A-013: 1310 nm) Output Power (Average): –4.0 dBm (Min.), +4.0 dBm (Max.), +7.0 dBm (Max.) (Non-modulation or input opened) Output Power Stability[*4]: ±0.02 dB Optical Modulation Amplitude[*3]: ≥–5.2 dBm Center Wavelength: 1290 nm (Min.), 1330 nm (Max.) Side Mode Suppression Ratio: ≥30 dB Extinction Ratio[*1, 2]: 2.0 to 6.0 dB, Steps: 0.1 dB VECP[*1, 2, 5, 6]: 1.47 dB (Min.), 2.2 dB (Max.) (In the Center 1% Region of the Eye, without noise input) 2.20 dB (Min.), 4.5 dB (Max.) (In the Center 1% Region of the Eye, noise input: 2.0 Vp-p, 100 MHz) Jitter[*1, 2, 6]: ≤0.25 UIp-p, Compliant with IEEE802.3-2005 Eye Mask[*1, 2, 6]: Compliant with IEEE802.3-2005 Clause 52 (10.3125 Gbit/s)
MU181620A-012/013	MU181620A-002/003	1550 nm Reference: MU181620A-002/003/012/013 (MU181620A-003/013: 1310 nm) Output Power (Average): –2.0 dBm (Min.), +4.0 dBm (Max.), +7.0 dBm (Max.) (Non-modulation or input opened) Output Power Stability[*4]: ±0.02 dB Center Wavelength: 1530 nm (Min.), 1565 nm (Max.) Side Mode Suppression Ratio: ≥30 dB Extinction Ratio[*1, 2]: 6.0 to 10.0 dB, Steps: 0.1 dB VECP[*1, 5]: ≤0.5 dB (In the Center 20% Region of the Eye) (Extinction Ratio: 9.0 dB, Use a reference O/E specified by Anritsu) Tr/Tf[*1, 3]: ≤30 ps (20 to 80%) Jitter[*1]: ≤0.2 UIp-p, Compliant with IEEE802.3-2005 Eye Mask[*2, 3]: Compliant with STM64/OC192 (9.95328 Gbit/s), IEEE802.3-2005 Clause 52 (10.3125 Gbit/s, Mask margin≥30%), STM64/OC192 with FEC (10.709 Gbit/s)
		1550 nm Stressed Eye: MU181620A-012/013 (MU181620A-013: 1310 nm) Output Power (Average): –2.0 dBm (Min.), +4.0 dBm (Max.), +7.0 dBm (Max.) (Non-modulation or input opened) Output Power Stability[*4]: ±0.02 dB Optical Modulation Amplitude[*3]: ≥–1.7 dBm Center Wavelength: 1530 nm (Min.), 1565 nm (Max.) Side Mode Suppression Ratio: ≥30 dB Extinction Ratio[*1, 2]: 2.0 to 5.0 dB, Steps: 0.1 dB VECP[*1, 2, 5, 7]: 1.8 dB (Min.), 2.7 dB (Max.) (In the Center 1% Region of the Eye, without noise input) 2.7 dB (Min.), 5.0 dB (Max.) (In the Center 1% Region of the Eye, noise input: 2.0 Vp-p, 100 MHz) Jitter[*1, 2, 7]: ≤0.25 UIp-p, Compliant with IEEE802.3-2005 Eye Mask[*1, 2, 7]: Compliant with IEEE802.3-2005 Clause 52 (10.3125 Gbit/s)
Fiber		SM Fiber (ITU-T G.652)
Connector		FC Connector (PC type) [MU181620A-037] SC Connector (PC type) [MU181620A-040] user-replaceable
Optical Attenuator		Output Power Control: –20.0 to –4.0 dBm, Steps: 0.01 dB (1310 nm) –20.0 to –2.0 dBm, Steps: 0.01 dB (1550 nm) Output Power Control Accuracy[*5]: ±0.5 dB (typ.) Attenuation Variable Setting Range: 0.0 to 16.0 dB, Steps: 0.01 dB (1310 nm) 0.0 to 18.0 dB, Steps: 0.01 dB (1550 nm) Attenuation Variable Setting Range Accuracy[*5]: ±0.5 dB (typ.)
Laser Safety[*9]		IEC 60825-1: 2007: CLASS 1 21CFR1040.10[*8]

● MU181640A Optical Receiver

Bit Rate	0.1 Gbit/s to 12.5 Gbit/s
Bandwidth	DC to 8.5 GHz (Bandwidth: –3 dB)
Optical Data Input	Signal Format: NRZ Wavelength: 750 nm to 1650 nm Maximum Input: +7 dBm (Peak), +2 dBm (Average), –2 dBm (Linear) (typ.) Return Loss: ≤–27 dB (SM), ≤–14 dB (MM) Sensitivity: –15.5 dBm (typ.) (10.3 Gbit/s, 1550 nm, SM, Extinction Ratio ≥10 dB) BER ≤10^{-12}: –15.5 dBm (typ.) (10.3 Gbit/s, 1310 nm, SM, Extinction Ratio ≥10 dB) –10.0 dBm (typ.) (10.3 Gbit/s, 850 nm, MM, Extinction Ratio ≥10 dB) Connector: FC Connector (PC type) [MU181640A-037] SC Connector (PC type) [MU181640A-040] User-replaceable Fiber: 10 µm/125 µm SM (ITU-T G.652), 50 µm/125 µm MM , 62.5 µm/125 µm MM
Data Output	Amplitude: 1550 nm, SM (≥150 mVp-p @–4 dBm, Extinction Ratio ≥10 dB) 1310 nm, SM (≥160 mVp-p @–4 dBm, Extinction Ratio ≥10 dB) 850 nm, MM (≥90 mVp-p @–4 dBm, Extinction Ratio ≥10 dB) Conversion Gain: 1550 nm, SM (≥400 V/W @–4 dBm) 1310 nm, SM (≥425 V/W @–4 dBm) 850 nm, MM (≥230 V/W @–4 dBm)

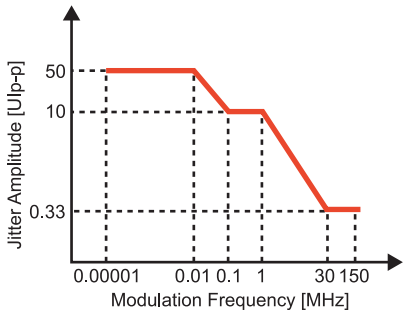
∗1: Bit Rate: 10.3125 Gbit/s
∗2: Use a filter of Bit Rate of 75%
∗3: Extinction Ratio: 10 dB
∗4: Stability level at one hour after a certain period of time after optical outputs
∗5: 20° to 30°C
∗6: Extinction Ratio: 3.5 dB
∗7: Extinction Ratio: 3.0 dB
∗8: Excludes deviations caused by conformance to Laser Notice No. 50 dated June 24, 2007
∗9: Safety measures for laser products
This product complies with optical safety standards in 21CFR1040.10 and IEC 60825-1; the following descriptive labels are affixed to the product.

- **MU183020A 28G/32G bit/s PPG, MU183021A 28G/32G bit/s 4ch PPG**

Bit Rate	Operational Bit-rate Range: 2.4 Gbit/s to 28.1 Gbit/s 2.4 Gbit/s to 32.1 Gbit/s (with Option-x01)
Bit-rate Setting Range (MU181000A/B synchronized operation)	This item is specified when MU181000A or MU181000B is installed into the same main frame. When Full Rate Clock Output is selected: 2.400 000 Gbit/s to 12.500 000 Gbit/s, 0.000 001 Gbit/s step 12.500 002 Gbit/s to 25.000 000 Gbit/s, 0.000 002 Gbit/s step 25.000 004 Gbit/s to 28.100 000 Gbit/s, 0.000 004 Gbit/s step 25.000 004 Gbit/s to 32.100 000 Gbit/s, 0.000 004 Gbit/s step (with Option-x01) When Half Rate Clock Output is selected: 2.400 000 Gbit/s to 25.000 000 Gbit/s, 0.000 002 Gbit/s step 25.000 004 Gbit/s to 28.100 000 Gbit/s, 0.000 004 Gbit/s step 25.000 004 Gbit/s to 32.100 000 Gbit/s, 0.000 004 Gbit/s step (with Option-x01)
Bit-rate Setting Range (MU181000A/B and MU181500B synchronized operation)	This item is specified when MU181000A and MU181500B are installed to the same main frame. When Full Rate Clock Output is selected: 2.400 000 Gbit/s to 3.125 000 Gbit/s, 0.000 001 Gbit/s step 3.200 001 Gbit/s to 6.250 000 Gbit/s, 0.000 001 Gbit/s step 6.400 001 Gbit/s to 12.500 000 Gbit/s, 0.000 001 Gbit/s step 12.800 002 Gbit/s to 25.000 000 Gbit/s, 0.000 002 Gbit/s step 25.600 004 Gbit/s to 28.100 000 Gbit/s, 0.000 004 Gbit/s step 25.600 004 Gbit/s to 32.100 000 Gbit/s, 0.000 004 Gbit/s step (with Option-x01) When Half Rate Clock Output is selected: 2.400 000 Gbit/s to 3.125 000 Gbit/s, 0.000 002 Gbit/s step 3.200 002 Gbit/s to 6.250 000 Gbit/s, 0.000 002 Gbit/s step 6.400 002 Gbit/s to 12.500 000 Gbit/s, 0.000 002 Gbit/s step 12.800 002 Gbit/s to 25.000 000 Gbit/s, 0.000 002 Gbit/s step 25.600 004 Gbit/s to 28.100 000 Gbit/s, 0.000 004 Gbit/s step 25.600 004 Gbit/s to 32.100 000 Gbit/s, 0.000 004 Gbit/s step (with Option-x01)
Bit-rate Setting Range (with external clock source)	This item is specified when external clock source is used. When Full Rate Clock Output is selected: 2.4 Gbit/s to 16.0 Gbit/s 16.0 Gbit/s to 20.4 Gbit/s 20.0 Gbit/s to 28.1 Gbit/s 20.0 Gbit/s to 32.1 Gbit/s (with Option-x01) When Half Rate Clock Output is selected: 2.4 Gbit/s to 28.1 Gbit/s 2.4 Gbit/s to 32.1 Gbit/s (with Option-x01)
Bit-rate Setting Range (MU181500B synchronized operation with external clock source)	This item is specified when MU181000B is installed into the same mainframe and external clock source is used. When Full Rate Clock Output is selected: 2.4 Gbit/s to 15.0 Gbit/s 15.0 Gbit/s to 20.0 Gbit/s 20.0 Gbit/s to 28.1 Gbit/s 20.0 Gbit/s to 30.0 Gbit/s (with Option-x01) 30.0 Gbit/s to 32.1 Gbit/s (with Option-x01) When Half Rate Clock Output is selected: 2.4 Gbit/s to 28.1 Gbit/s 2.4 Gbit/s to 30.0 Gbit/s (with Option-x01) 30.0 Gbit/s to 32.1 Gbit/s (with Option-x01)

External Clock Input	Number of Input: 1 (Single end) Frequency: 1.2 GHz to 16.05 GHz Amplitude: 0.3 Vp-p to 1.0 Vp-p (–6.5 to +4.0 dBm) Termination: 50Ω/AC Coupling Connector: SMA (f.)
Aux Input	Number of Input: 1 (Single end) Signal Type: Error Injection, Burst Minimum Pulse Width: 1/128 Input level: 0/–1 V (H: –0.25 V to 0.05 V, L: –1.1 V to –0.8 V) Termination: 50Ω/GND Connector: SMA (f.)
Aux Output	Number of Output: 2 (Differential) Signal Type: 1/n Clock (n = 4, 6, 8, 10 · · · 510, 512), Pattern Sync, Burst Out2 Output level: 0/–0.6 V (H: –0.25 V to 0.05 V, L: –0.80 V to –0.45 V) Termination: 50Ω/GND Connector: SMA (f.)
Gating Output	Burst, Repeat Timing Signal Output level: 0/–1 V (H: –0.25 V to 0.05 V, L: –1.25 V to –0.8 V) Termination: 50Ω/GND Connector: SMA (f.)
Pattern Generation	PRBS Pattern length: 2^n – 1 (n = 7, 9, 10, 11, 15, 20, 23, 31) Mark ratio: 1/2 (1/2INV is supported by a logic inversion) Zero-Substitution: Pattern with continuous 0 s appended to M-sequence signal + 1 bit Pattern: 2^n or 2^n – 1 (n = 7, 9, 10, 11, 15, 20, 23) 0 continuous substitution count: 1 to (pattern length – 1) bits 0 at next bit after 0 substitution changed to 1 Data Data length: 2 bits to 268 435 456 bits, 1 bit step Mixed Pattern Pattern: PRBS, Data – 1 to Data – 511 Mixed Row Length (Data + PRBS Length): 1 536 to 2 415 919 104, 256 bits step Data length: 1 024 bits to 268 435 456 bits, 1 bit step PRBS length/Mark Ratio: Same as PRBS PRBS Sequence: Restart, Consecutive
Pattern Sequence	Repeat: Continuous Pattern Burst Burst Cycle: 25 600 bits to 2 147 483 648 bits, 256 bits step Enable period Internal: 12 800 bits to 2 147 483 392 bits, 256 bits step Ext Trigger, Enable: 12 800 bits to 2 147 483 648 bits, 256 bits step
Pre-code	Pre-code function: ON and OFF Type: DQPSK (MU183020A, MU183021A) DP-QPSK (MU183021A) Initial Data: 0 or 1 selectable
Error addition	Timing: Internal, external trigger Error event: Repeat, Single Error rate: a × 10^{-b} (a = 1 to 9, b = 3 to 12), Upper limit: 5E-3

<table>
<tr><td>Data Output[*1]</td><td>
<table>
<tr><th></th><th>MU183020A-x12</th><th>MU183020A-x13</th><th>MU183021A-x22</th><th>MU183021A-x23</th></tr>
<tr><td>Number of Outputs</td><td colspan="2">2: Data, XData (Independent)</td><td colspan="2">4: Data1, XData1, Data2, XData2 (Independent)</td></tr>
<tr><td>Output Amplitude</td><td>0.5 Vp-p to 2.0 Vp-p
2 mV step</td><td>0.5 Vp-p to 3.5 Vp-p
2 mV step</td><td>0.5 Vp-p to 2.0 Vp-p
2 mV step</td><td>0.5 Vp-p to 3.5 Vp-p
2 mV step</td></tr>
</table>
<table>
<tr><th></th><th>MU183021A-x12</th><th>MU183021A-x13</th></tr>
<tr><td>Number of Outputs</td><td colspan="2">8: Data, XData (Independent)</td></tr>
<tr><td>Output Amplitude</td><td>0.5 Vp-p to 2.0 Vp-p
2 mV step</td><td>0.5 Vp-p to 3.5 Vp-p
2 mV step</td></tr>
</table>
Output amplitude setting error: ±50 mV ±17% of setting amplitude[*2]
Offset: –2.0 Voh to +3.3 Voh, 1 mV step
Current limitation: Sourcing 50 mA, Sinking 80 mA
Cross point setting range:
20 to 80%/0.1% step: at 1.0 Vp-p to upper limit of output amplitude setting
30 to 70%/0.1% step: at 0.5 Vp-p to 0.998 Vp-p
Tr/Tf 12 ps (20 to 80%)[*3, *4, *5]
Jitter (p-p): 8 ps p-p[*3, *4, *5, *6, *10]
Jitter (RMS): 700 fs[*3, *4, *5, *6]
Waveform Distortion (0-peak): ±25 mV ±15%[*3, *4, *5]
Output: On/Off selectable
Inter channel skew: ±0.25 UI[*6, *7, *8]
Termination: AC/DC 50Ω
Connector: K (f.)
</td></tr>
<tr><td>Clock Output[*9]</td><td>
Number of output: 1
Full Rate : Clock frequency is same as bit-rate when Full Rate Clock Output is selected.
2.4 GHz to 28.1 GHz
2.4 GHz to 32.1 GHz (Option-x01)
Half Rate: Clock frequency is half of bit-rate when Half Rate Clock Output is selected.
1.2 GHz to 14.05 GHz
1.2 GHz to 16.05 GHz (Option-x01)
Amplitude: 0.3 Vp-p to 1.0 Vp-p
Output: On/Off selectable
Termination: 50Ω/AC Coupling
Connector: K (f.)
</td></tr>
<tr><td>Delay
(MU183020A-x30, x31
MU183021A-x30)</td><td>
Phase variable range: –1 000 mUI to +1 000 mUI, 2 mUI step
Phase setting error: ±50 mUIp-p[*5, *6] (Bit rate ≤28.1 Gbit/s), ±75 mUIp-p[*5, *6] (Bit rate >28.1 Gbit/s)
</td></tr>
</table>

Jitter Tolerance	Bit-rate: 28.1 Gbit/s 32.1 Gbit/s (Option-x01) Test Pattern: PRBS $2^{31} - 1$ 
Multi-Channel Operation	MU183020A Combination*11, *12: 2ch (Bit shifted test pattern as 56G/64G bit/s band signal source) CH Sync.: 2 to 4ch*13, *16 Phase variable range: –64 000 mUI to +64 000 mUI*15 MU183021A Combination*12: 2ch (Bit shifted test pattern as 56G/64G bit/s band signal source) 4ch (Bit shifted test pattern as 112G/128G bit/s band signal source) CH Sync.: 2 to 8ch*13, *14 Phase variable range: –64 000 mUI to +64 000 mUI*15
Operating Temperature	15° to 35°C

∗1: Unless otherwise specified , these are defined with PRBS$2^{31} - 1$, Mark Ratio 1/2, Cross-point 50%, using an optional accessories (J1439A coaxial cable, 0.8 m, K connector) and a sampling oscilloscope which has 70 GHz bandwidth.
∗2: This value is assured when Cross point is set to 50% or within the range of 30 to 80% and Bit rate is set to 25 or 28.1 Gbit/s.
∗3: Without Option-x01: at 28.1 Gbit/s
With Option-x01: at 32.1 Gbit/s
∗4: With Option-x12 or x22: at amplitude 2.0 Vp-p,
With Option-x13 or x23: at amplitude 3.5 Vp-p
∗5: Typical value
∗6: Using oscilloscope with intrinsic jitter of less than 200 fs (RMS).
∗7: With MU183020A-x22 or MU183020A-x23. Or, when MU183021A is used.
∗8: With Option-x30 or x31.
∗9: These values are monitored using an applicable part (J1439A coaxial cable, 0.8 m, K connector) at a sampling oscilloscope bandwidth of 70 GHz.
∗10: This value is the peak-to-peak jitter of the crossing point on EYE pattern measured at 1k Jitter total samples and 30 counts, and is not the estimated TJ at BER 1E-12 using DR/RJ decomposition.
∗11: Option-x31 is required for target channels.
∗12: Combination extending over multiple slots cannot be set.
∗13: When target channels are installed successively from Slot 1.
∗14: Option-x30 is required for target channels.
∗15: A separate value can be set for each channel. This value is common to both Channel Combination and Channel Synchronization.
∗16: Option-x30 or x31 is required for target channels.

• MU183040A 28G/32G bit/s ED, MU183041A 28G/32G bit/s 4ch ED

Bit-rate	Operational Bit-rate Range: 2.4 Gbit/s to 28.1 Gbit/s 2.4 Gbit/s to 32.1 Gbit/s (with Option-x01)
Data Input	Number of Input MU183040A-010 · · · 2 (Data , XData) MU183040A-020 · · · 4 (Data1 to Data2, XData1 to XData2) MU183041A · · · 8 (Data1 to Data4, XData1 to XData4) Amplifier: Single-ended 50Ω, Differential 50Ω, Differential 100Ω can be set. Data, XData can be set. Tracking, Independent, Alternate can be set. (Data-XData or XData-Data can be set when Alternate is selected.*1) Format: NRZ Amplitude: 0.25 Vp-p to 2.0 Vp-p Threshold voltage: –3.5 V to +3.3 V, 1 mV step (Can be set individually for Data and XData.) Absolute value of difference between Data and XData Threshold values shall be 3 V or less. Sensitivity: 50 mVp-p*2, *3, *4 Phase Margin: 20 ps*2, *4, *5, *7 28 ps*4, *5, *6, *7 Termination: GND/50Ω, Variable/50Ω Termination voltage: –2.5 V to +3.5 V, 10 mV step (When termination variable is selected) Connector: K (f.)
Clock Input	Number of Input: 1 (Single-end) Frequency: 1.2 GHz to 16.05 GHz Amplitude: 0.3 Vp-p to 1.0 Vp-p (–6.5 to +4.0 dBm) Termination: 50Ω/AC Coupling Connector: SMA (f.)
Aux Input	Number of Input: 1 (Single-end) Input Signal: External Mask, Burst Minimum Pulse Width: 1/128 of Bit-rate Input Level: 0/–1 V (H: –0.25 V to 0.05 V, L: –1.1 V to –0.8 V) Termination: GND/50Ω Connector: SMA (f.)
Aux Output	Number of Output: 2 (Differential) Input Signal: 1/n Clock (n = 4, 6, 8, 10 · · · 510, 512), Pattern Sync, Error, Sync. gain Pattern Sync. PRBS, PRGM: Position: (Least common multiple of 1 to Pattern Length and 128) − 135, 8 step Mixed Data: Block No. setting: 1 to the Block No. specified for Mixed Data, in single steps Row No. setting: 1 to the Row No. specified for Mixed Data, in single steps Output Level: 0/–0.6 V (H: –0.25 V to 0.05 V, L: –0.80 V to –0.45 V) Termination: GND/50Ω Connector: SMA (f.)

Pattern Detection	PRBS Pattern length: 2^n – 1 (n = 7, 9, 10, 11, 15, 20, 23, 31) Mark ratio: 1/2 (1/2INV is supported by a logic inversion) Zero-Substitution: Pattern with continuous 0 s appended to M-sequence signal + 1 bit Pattern: 2^n or 2^n – 1 (n = 7, 9, 10, 11, 15, 20, 23) 0 continuous substitution count: 1 to (pattern length – 1) bits 0 at next bit after 0 substitution changed to 1 Data Data length: 2 bits to 268 435 456 bits, 1 bit step Mixed Pattern Pattern: PRBS, Data – 1 to Data – 511 Mixed Row Length (Data + PRBS Length): 1 536 to 2 415 919 104, 256 bits step Data length: 1 024 bits to 268 435 456 bits, 1 bit step PRBS length/Mark Ratio: Same as PRBS PRBS Sequence: Restart, Consecutive
Pattern Sequence	Repeat: Continuous Pattern Burst Burst Cycle: 25 600 bits to 2 147 483 648 bits, 256 bits step Enable period Internal: 12 800 bits to 2 147 483 392 bits, 256 bits step Ext Trigger, Enable: 12 800 bits to 2 147 483 648 bits, 256 bits step
Measurement Type	Error Rate, Error Count, Error Interval, Error Free Interval (%), Frequency Clock Count, Sync Loss Interval, Clock Loss Interval
Error Detection Mode	Total error, Insertion Error, Omission Error, Transition Error, Non Transition Error
Error Analysis	Eye Margin, Eye Diagram, Bathtub Jitter, Auto Adjust, Auto Search
Burst Measurement Signal	Burst Trigger: Internal, External
Variable Clock Delay	Phase variable range: –1 000 mUI to +1 000 mUI, 2 mUI step Phase setting error: ±50 mUIp-p*4, *8 mUI - ps selectable
Multi-channel Operation	MU183040A (with Option-x20): 2ch combination*9 MU183041A (4ch): 2ch or 4ch combination
Operating Temperature	15° to 35°C

∗1: Absolute value of difference between Data and XData Threshold values shall be 1.5 V or less.
∗2: 28.1 Gbit/s
∗3: PRBS31, Single-ended, Mark Ratio 1/2, 20° to 30°C
∗4: Typical value
∗5: 0.5 Vp-p Input
∗6: 25 Gbit/s
∗7: PRBS31, Single-ended, Mark Ratio 1/2
∗8: Using oscilloscope with residual jitter of less than 200 fs (RMS).
∗9: Combination extending over multiple slots cannot be set.

Ordering Information

Please specify the model/order number, name and quantity when ordering.
The names listed in the chart below are Order Names. The actual name of the item may differ from the Order Name.

● MP1800A

Model/Order No.	Name	
Main Frame		
MP1800A	Signal Quality Analyzer	
Standard Accessories		
J0491	Shield Power Cord (13A):	1 pc
Z0306A	Wrist Strap:	1 pc
Z0541A	USB Mouse:	1 pc
B0329G	Front Cover for 3/4MW 4U:	1 pc
B0574A	MP1800A Protect Cover:	1 pc
MX180000A	Signal Quality Analyzer Control Software:	1 pc
Z0897A	MP1800A Manual CD:	1 pc
Options		
MP1800A-001	GPIB	
MP1800A-002	LAN	
MP1800A-014	2-Slot for PPG and/or ED	
MP1800A-015	4-Slot for PPG and/or ED	
MP1800A-016	6-Slot for PPG and/or ED	
Retrofit Options		
MP1800A-101	GPIB Retrofit	
MP1800A-102	LAN Retrofit	
Calibration Service		
MP1800A-190	25G Calibration of PPG and MUX Retrofit	
Maintenance Service		
MP1800A-ES310	Three Years Extended Warranty Service	
MP1800A-ES510	Five Years Extended Warranty Service	

● MT1810A

Model/Order No.	Name	
Main Frame		
MT1810A	4 Slot Chassis	
Standard Accessories		
J0491	Shield Power Cord (13A):	1 pc
Z0306A	Wrist Strap:	1 pc
J1109B	LAN Cable (CAT5, Cross), 5 m:	1 pc
B0575A	MT1810A Protect Cover:	1 pc
MX180000A	Signal Quality Analyzer Control Software:	1 pc
Z0897A	MP1800A Manual CD:	1 pc
Options		
MT1810A-014	2-Slot for PPG and/or ED	
MT1810A-015	4-Slot for PPG and/or ED	
Calibration Service		
MT1810A-190	25G PPG/MUX Calibration Retrofit	
Maintenance Service		
MT1810A-ES310	Three Years Extended Warranty Service	
MT1810A-ES510	Five Years Extended Warranty Service	

● MU181000A

Model/Order No.	Name	
Unit/Module		
MU181000A	12.5 GHz Synthesizer	
Standard Accessories		
J1349A	Coaxial Cable 0.3 m (SMA, DC to 18 GHz):	1 pc
Options		
MU181000A-001	Jitter Modulation	
Retrofit Options		
MU181000A-101	Jitter Modulation Retrofit	
Maintenance Service		
MU181000A-ES310	Three Years Extended Warranty Service	
MU181000A-ES510	Five Years Extended Warranty Service	

● MU181000B

Model/Order No.	Name	
Unit/Module		
MU181000B	12.5 GHz 4port Synthesizer	
Standard Accessories		
J1349A	Coaxial Cable 0.3 m (SMA, DC to 18 GHz):	4 pcs
Options		
MU181000B-001	Jitter Modulation	
Retrofit Options		
MU181000B-101	Jitter Modulation Retrofit	
Maintenance Service		
MU181000B-ES310	Three Years Extended Warranty Service	
MU181000B-ES510	Five Years Extended Warranty Service	

● MU181500B

Model/Order No.	Name	
Unit/Module		
MU181500B	Jitter Modulation Source	
Standard Accessories		
J1349A	Coaxial Cable 0.3 m (SMA, DC to 18 GHz):	1 pc
J1508A	BNC-SMA Connector Cable (30 cm):	2 pcs
Maintenance Service		
MU181500B-ES310	Three Years Extended Warranty Service	
MU181500B-ES510	Five Years Extended Warranty Service	

● MU181800A

Model/Order No.	Name
Unit/Module	
MU181800A	12.5 GHz Clock Distributor
Maintenance Service	
MU181800A-ES310	Three Years Extended Warranty Service
MU181800A-ES510	Five Years Extended Warranty Service

● MU181800B

Model/Order No.	Name
Unit/Module	
MU181800B	14 GHz Clock Distributor
Maintenance Service	
MU181800B-ES310	Three Years Extended Warranty Service
MU181800B-ES510	Five Years Extended Warranty Service

● MU181020A

Model/Order No.	Name	
Unit/Module		
MU181020A	12.5 Gbit/s PPG	
Standard Accessories		
J1137	Terminator (50Ω):	3 pcs
J1341A	Open:	1 pc
Options		
MU181020A-001	9.8 to 12.5 Gbit/s	
MU181020A-002	0.1 to 12.5 Gbit/s	
MU181020A-010	Variable Data Output (0.05 to 0.8 Vp-p)	
MU181020A-011	Variable Data Output (0.25 to 2.5 Vp-p)	
MU181020A-012	High Performance Data Output (0.05 to 2.0 Vp-p)	
MU181020A-013	Variable Data Output (0.5 to 3.5 Vp-p)	
MU181020A-021	Differential Clock Output (0.1 to 2.0 Vp-p)	
MU181020A-030	Variable Data Delay	
Retrofit Options		
MU181020A-110	Variable Data Output (0.05 to 0.8 Vp-p) Retrofit	
MU181020A-111	Variable Data Output (0.25 to 2.5 Vp-p) Retrofit	
MU181020A-112	High Performance Data Output (0.05 to 2.0 Vp-p) Retrofit	
MU181020A-113	Variable Data Output (0.5 to 3.5 Vp-p) Retrofit	
MU181020A-121	Differential Clock Output (0.1 to 2.0 Vp-p) Retrofit	
MU181020A-130	Variable Data Delay Retrofit	
Standard Accessories for MU181020A-011/111		
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2 pcs
Standard Accessories for MU181020A-012/112		
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2 pcs
Standard Accessories for MU181020A-013/113		
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2 pcs
Standard Accessories for MU181020A-021/121		
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2 pcs
J1137	Terminator (50Ω):	1 pc
Maintenance Service		
MU181020A-ES310	Three Years Extended Warranty Service	
MU181020A-ES510	Five Years Extended Warranty Service	

● MU181020B

Model/Order No.	Name	
Unit/Module		
MU181020B	14 Gbit/s PPG	
Standard Accessories		
J1137	Terminator (50Ω):	3 pcs
J1341A	Open:	1 pc
Options		
MU181020B-002	0.1 to 14 Gbit/s	
MU181020B-003	14.05 Gbit/s Extension	
MU181020B-011	Variable Data Output (0.25 to 2.5 Vp-p)	
MU181020B-012	High Performance Data Output (0.05 to 2.0 Vp-p)	
MU181020B-013	Variable Data Output (0.5 to 3.5 Vp-p)	
MU181020B-021	Differential Clock Output (0.1 to 2.0 Vp-p)	
MU181020B-030	Variable Data Delay	
Retrofit Options		
MU181020B-111	Variable Data Output (0.25 to 2.5 Vp-p) Retrofit	
MU181020B-112	High Performance Data Output (0.05 to 2.0 Vp-p) Retrofit	
MU181020B-113	Variable Data Output (0.5 to 3.5 Vp-p) Retrofit	
MU181020B-121	Differential Clock Output (0.1 to 2.0 Vp-p) Retrofit	
MU181020B-130	Variable Data Delay Retrofit	
Standard Accessories for MU181020B-011/111		
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2 pcs
Standard Accessories for MU181020B-012/112		
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2 pcs
Standard Accessories for MU181020B-013/113		
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2 pcs
Standard Accessories for MU181020B-021/121		
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2 pcs
J1137	Terminator (50Ω):	1 pc
Maintenance Service		
MU181020B-ES310	Three Years Extended Warranty Service	
MU181020B-ES510	Five Years Extended Warranty Service	

● MU181040A

Model/Order No.	Name	
Unit/Module		
MU181040A	12.5 Gbit/s ED	
Options		
MU181040A-001	9.8 to 12.5 Gbit/s	
MU181040A-002	0.1 to 12.5 Gbit/s	
MU181040A-020	Clock Recovery	
MU181040A-030	Variable Clock Delay	
Retrofit Options		
MU181040A-120	Clock Recovery Retrofit	
MU181040A-130	Variable Clock Delay Retrofit	
Standard Accessories for MU181040A-001		
J1341A	Open:	2 pcs
Standard Accessories for MU181040A-002		
J1341A	Open:	3 pcs
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2 pcs
J1137	Terminator (50Ω):	2 pcs
Standard Accessories for MU181040A-020/120		
J1137	Terminator (50Ω):	1 pc
Maintenance Service		
MU181040A-ES310	Three Years Extended Warranty Service	
MU181040A-ES510	Five Years Extended Warranty Service	

● MU181040B

Model/Order No.	Name	
Unit/Module		
MU181040B	14 Gbit/s ED	
Options		
MU181040B-002	0.1 to 14 Gbit/s	
MU181040B-003	14.05 Gbit/s Extension	
MU181040B-020	Clock Recovery	
MU181040B-030	Variable Clock Delay	
Retrofit Options		
MU181040B-120	Clock Recovery Retrofit	
MU181040B-130	Variable Clock Delay Retrofit	
Standard Accessories for MU181040B-002		
J1341A	Open:	3 pcs
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2 pcs
J1137	Terminator (50Ω):	2 pcs
Standard Accessories for MU181040B-020/120		
J1137	Terminator (50Ω):	1 pc
Maintenance Service		
MU181040B-ES310	Three Years Extended Warranty Service	
MU181040B-ES510	Five Years Extended Warranty Service	

● MU182020A

Model/Order No.	Name	
Unit/Module		
MU182020A	25 Gbit/s 1ch MUX	
Standard Accessories		
J1137	Terminator (50 Ω):	5 pcs
J1341A	Open:	4 pcs
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2 pcs
	MU182020A Semi-Rigid Cable Set (MUX-PPG):	1 pc
Options		
MU182020A-001	28 Gbit/s Extension	
MU182020A-002	Clock Input Band Switch	
MU182020A-003	28.1 Gbit/s Extension	
MU182020A-010	Variable Data Output (0.25 to 1.75 Vp-p)	
MU182020A-011	Variable Data Output (0.5 to 2.5 Vp-p)	
MU182020A-013	Variable Data Output (0.5 to 3.5 Vp-p)	
MU182020A-021	Variable Clock Output (0.5 to 2.0 Vp-p)	
MU182020A-030	25 Gbit/s Variable Data Delay	
MU182020A-031	28 Gbit/s Variable Data Delay	
Retrofit Options		
MU182020A-101	28 Gbit/s Extension Retrofit	
MU182020A-102	Clock Input Band Switch Retrofit	
MU182020A-110	Variable Data Output (0.25 to 1.75 Vp-p) Retrofit	
MU182020A-111	Variable Data Output (0.5 to 2.5 Vp-p) Retrofit	
MU182020A-113	Variable Data Output (0.5 to 3.5 Vp-p) Retrofit	
MU182020A-121	Variable Clock Output (0.5 to 2.0 Vp-p) Retrofit	
MU182020A-130	25 Gbit/s Variable Data Delay Retrofit	
MU182020A-131	28 Gbit/s Variable Data Delay Retrofit	
Standard Accessories for MU182020A-002/102		
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2 pcs
Standard Accessories for MU182020A-020/120		
J1359A	Coaxial Adapter (K-P, K-J, SMA):	1 pc
Maintenance Service		
MU182020A-ES310	Three Years Extended Warranty Service	
MU182020A-ES510	Five Years Extended Warranty Service	

● MU182040A

Model/Order No.	Name	
Unit/Module		
MU182040A	25 Gbit/s 1ch DEMUX	
Standard Accessories		
J1137	Terminator (50 Ω):	4 pcs
J1341A	Open:	3 pcs
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2 pcs
	MU182040A Semi-Rigid Cable Set (DEMUX-ED):	1 pc
Options		
MU182040A-001	28 Gbit/s Extension	
MU182040A-002	Clock Input Band Switch	
MU182040A-003	28.1 Gbit/s Extension	
MU182040A-030	25 GHz Variable Clock Delay	
MU182040A-031	28 GHz Variable Clock Delay	
Retrofit Options		
MU182040A-101	28 Gbit/s Extension Retrofit	
MU182040A-102	Clock Input Band Switch Retrofit	
MU182040A-130	25 GHz Variable Clock Delay Retrofit	
MU182040A-131	28 GHz Variable Clock Delay Retrofit	
Standard Accessories for MU182040A-002/102		
J1359A	Coaxial Adapter (K-P, K-J, SMA):	1 pc
Maintenance Service		
MU182040A-ES310	Three Years Extended Warranty Service	
MU182040A-ES510	Five Years Extended Warranty Service	

● MU182021A

Model/Order No.	Name	
Unit/Module		
MU182021A	25 Gbit/s 2ch MUX	
Standard Accessories		
J1137	Terminator (50 Ω):	9 pcs
J1341A	Open:	6 pcs
J1359A	Coaxial Adapter (K-P, K-J, SMA):	4 pcs
	MU182021A Semi-Rigid Cable Set (MUX-PPG):	1 pc
Options		
MU182021A-001	28 Gbit/s Extension	
MU182021A-002	Clock Input Band Switch	
MU182021A-003	28.1 Gbit/s Extension	
MU182021A-010	Variable Data Output (0.25 to 1.75 Vp-p)	
MU182021A-011	Variable Data Output (0.5 to 2.5 Vp-p)	
MU182021A-013	Variable Data Output (0.5 to 3.5 Vp-p)	
MU182021A-021	Differential Clock Output (0.5 to 2.0 Vp-p)	
MU182021A-030	25 Gbit/s Variable Data Delay	
MU182021A-031	28 Gbit/s Variable Data Delay	
MU182021A-040	Emphasis Control	
Retrofit Options		
MU182021A-101	28 Gbit/s Extension Retrofit	
MU182021A-102	Clock Input Band Switch Retrofit	
MU182021A-110	Variable Data Output (0.25 to 1.75 Vp-p) Retrofit	
MU182021A-111	Variable Data Output (0.5 to 2.5 Vp-p) Retrofit	
MU182021A-113	Variable Data Output (0.5 to 3.5 Vp-p) Retrofit	
MU182021A-121	Differential Clock Output (0.5 to 2.0 Vp-p) Retrofit	
MU182021A-130	25 Gbit/s Variable Data Delay Retrofit	
MU182021A-131	28 Gbit/s Variable Data Delay Retrofit	
MU182021A-140	Emphasis Control Retrofit	
Standard Accessories for MU182021A-002/102		
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2 pcs
Standard Accessories for MU182021A-021/121		
J1359A	Coaxial Adapter (K-P, K-J, SMA):	1 pc
Maintenance Service		
MU182021A-ES310	Three Years Extended Warranty Service	
MU182021A-ES510	Five Years Extended Warranty Service	

● MU182041A

Model/Order No.	Name	
Unit/Module		
MU182041A	25 Gbit/s 2ch DEMUX	
Standard Accessories		
J1137	Terminator (50 Ω):	8 pcs
J1341A	Open:	5 pcs
J1359A	Coaxial Adapter (K-P, K-J, SMA):	4 pcs
	MU182041A Semi-Rigid Cable Set (DEMUX-ED):	1 pc
Options		
MU182041A-001	28 Gbit/s Extension	
MU182041A-002	Clock Input Band Switch	
MU182041A-003	28.1 Gbit/s Extension	
MU182041A-030	25 GHz Variable Clock Delay	
MU182041A-031	28 GHz Variable Clock Delay	
Retrofit Options		
MU182041A-101	28 Gbit/s Extension Retrofit	
MU182041A-102	Clock Input Band Switch Retrofit	
MU182041A-130	25 GHz Variable Clock Delay Retrofit	
MU182041A-131	28 GHz Variable Clock Delay Retrofit	
Standard Accessories for MU182041A-002/102		
J1359A	Coaxial Adapter (K-P, K-J, SMA)	1 pc
Maintenance Service		
MU182041A-ES310	Three Years Extended Warranty Service	
MU182041A-ES510	Five Years Extended Warranty Service	

• MU183020A

Model/Order No.	Name	
Unit/Module		
MU183020A	28G/32G bit/s PPG	
Standard Accessories		
J1137	Terminator:	3 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	1 pc
J1341A	Open:	1 pc
J1451A	Coaxial Attenuator (6 dB):	1 pc
Z0897A	MP1800A Manual CD:	1 pc
Z0918A	MX180000A Software CD:	1 pc
Options		
MU183020A-001	32G bit/s Extension	
MU183020A-012	1ch 2 V Data Output	
MU183020A-013	1ch 3.5 V Data Output	
MU183020A-022	2ch 2 V Data Output	
MU183020A-023	2ch 3.5 V Data Output	
MU183020A-030	1ch Data Delay	
MU183020A-031	2ch Data Delay	
Retrofit Options		
MU183020A-101	32G bit/s Extension Retrofit	
MU183020A-112	1ch 2 V Data Output Retrofit	
MU183020A-113	1ch 3.5 V Data Output Retrofit	
MU183020A-122	2ch 2 V Data Output Retrofit	
MU183020A-123	2ch 3.5 V Data Output Retrofit	
MU183020A-130	1ch Data Delay Retrofit	
MU183020A-131	2ch Data Delay Retrofit	
Standard Accessories for MU183020A-x12, x13		
J1137	Terminator:	2 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	2 pcs
Standard Accessories for MU183020A-x22, x23		
J1137	Terminator:	4 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	4 pcs
Maintenance Service		
MU183020A-ES310	Three Years Extended Warranty Service	
MU183020A-ES510	Five Years Extended Warranty Service	

• MU183040A

Model/Order No.	Name	
Unit/Module		
MU183040A	28G/32G bit/s ED	
Standard Accessories		
J1137	Terminator:	2 pcs
J1341A	Open:	1 pc
Z0897A	MP1800A Manual CD:	1 pc
Z0918A	MX180000A Software CD:	1 pc
Options		
MU183040A-001	32G bit/s Extension	
MU183040A-010	1ch ED	
MU183040A-020	2ch ED	
Retrofit Options		
MU183040A-101	32G bit/s Extension Retrofit	
MU183040A-120	2ch ED Retrofit	
Standard Accessories for MU183021A-x10		
J1341A	Open:	2 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	2 pcs
Standard Accessories for MU183040A-x20		
J1341A	Open:	4 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	4 pcs
Maintenance Service		
MU183040A-ES310	Three Years Extended Warranty Service	
MU183040A-ES510	Five Years Extended Warranty Service	

• MU183021A

Model/Order No.	Name	
Unit/Module		
MU183021A	28G/32G bit/s 4ch PPG	
Standard Accessories		
J1137	Terminator:	3 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	1 pc
J1341A	Open:	1 pc
Z0897A	MP1800A Manual CD:	1 pc
Z0918A	MX180000A Software CD:	1 pc
Options		
MU183021A-001	32G bit/s Extension	
MU183021A-012	4ch 2.0 V Data Output	
MU183021A-013	4ch 3.5 V Data Output	
MU183021A-030	4ch Data Delay	
Retrofit Options		
MU183021A-101	32G bit/s Extension Retrofit	
MU183021A-112	4ch 2.0 V Data Output Retrofit	
MU183021A-113	4ch 3.5 V Data Output Retrofit	
MU183021A-130	4ch Data Delay Retrofit	
Standard Accessories for MU183021A-x12, x13		
J1137	Terminator:	8 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	8 pcs
Maintenance Service		
MU183021A-ES310	Three Years Extended Warranty Service	
MU183021A-ES510	Five Years Extended Warranty Service	

• MU183041A

Model/Order No.	Name	
Unit/Module		
MU183041A	28G/32G bit/s 4ch ED	
Standard Accessories		
J1137	Terminator:	3 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA):	1 pcs
J1341A	Open:	1 pc
Z0897A	MP1800A Manual CD:	1 pc
Z0918A	MX180000A Software CD:	1 pc
Options		
MU183041A-001	32G bit/s Extension	
Retrofit Options		
MU183041A-101	32G bit/s Extension Retrofit	
Maintenance Service		
MU183041A-ES310	Three Years Extended Warranty Service	
MU183041A-ES510	Five Years Extended Warranty Service	

• MU181600A

Model/Order No.	Name	
Unit/Module		
MU181600A*1	Optical Transceiver (XFP)	
Standard Accessories		
J1355A	Semirigid Cable:	1 pc
J0541E	6 dB Fixed Attenuator:	2 pcs
J0541A	10 dB Fixed Attenuator:	2 pcs
Maintenance Service		
MU181600A-ES310	Three Years Extended Warranty Service	
MU181600A-ES510	Five Years Extended Warranty Service	

• MU181601A

Model/Order No.	Name	
Unit/Module		
MU181601A*2	Optical Transceiver (SFP)	
Standard Accessories		
J0541E	6 dB Fixed Attenuator:	1 pc
Maintenance Service		
MU181601A-ES310	Three Years Extended Warranty Service	
MU181601A-ES510	Five Years Extended Warranty Service	

• MU181620A

Model/Order No.	Name	
Unit/Module		
MU181620A	Stressed Eye Transmitter	
Options		
MU181620A-001	1310 nm Reference	
MU181620A-002	1550 nm Reference	
MU181620A-003	1310 nm/1550 nm Reference	
MU181620A-011	1310 nm Stressed Eye	
MU181620A-012	1550 nm Stressed Eye	
MU181620A-013	1310 nm/1550 nm Stressed Eye	
MU181620A-037	FC Connector	
MU181620A-040	SC Connector	
Standard Accessories for MU181620A-011/012/013		
J1137	Terminator (50 Ω):	1 pc
Standard Accessories for MU181620A-011/013		
J1404A	Semirigid Cable:	1 pc
Standard Accessories for MU181620A-012/013		
J1405A	Semirigid Cable:	1 pc
Maintenance Service		
MU181620A-ES310	Three Years Extended Warranty Service	
MU181620A-ES510	Five Years Extended Warranty Service	

• MU181640A

Model/Order No.	Name	
Unit/Module		
MU181640A	Optical Receiver	
Options		
MU181640A-004	Band Width 8.5 GHz	
MU181640A-037	FC Connector	
MU181640A-040	SC Connector	
Standard Accessories		
J1359A	Coaxial Adapter (K-P, K-J, SMA):	1 pc
Maintenance Service		
MU181640A-ES310	Three Years Extended Warranty Service	
MU181640A-ES510	Five Years Extended Warranty Service	

• Software

Model/Order No.	Name
MX180000A	Signal Quality Analyzer Control Software
MX180000A-001	Pre-Code
MX180000A-002	De-Code
MX180001A	SDH/SONET Pattern Editor
MX180002A	Stressed Eye Measurement Control Software
MX180003A	GbE/10 GbE Pattern Editor
MX180004A	PON Application Software
MX180005A	Jitter Application Software
MX181500A	Jitter/Noise Tolerance Test Software

• Optional Accessories

Model/Order No.	Name
J0008	GPIB Cable 2 m
J1137	Terminator (50 Ω)
J1341A	Open
J1342A	Coaxial Cable 0.8 m (APC-3.5, DC to 27.5 GHz)
J1343A	Coaxial Cable 1.0 m (SMA, DC to 18 GHz)
J1349A	Coaxial Cable 0.3 m (SMA, DC to 18 GHz)
J1439A	Coaxial Cable 0.8 m (K connector) (DC to 40 GHz)
G0174A	850 nm XFP Module (9.95 to 11.10 Gbit/s)
G0175A	1310 nm XFP Module (9.95 to 11.30 Gbit/s)
G0176A	1550 nm XFP Module (9.95 to 10.75 Gbit/s)
G0177A	850 nm SFP Module (1.062 to 4.25 Gbit/s)
G0178A	1310 nm SFP Module (0.155 to 2.67 Gbit/s)
G0179A	1550 nm SFP Module (0.155 to 2.67 Gbit/s)
J0617B	Replaceable Optical Connector (FC-PC)
J0619B	Replaceable Optical Connector (SC)
J0635A	FC•PC-FC•PC-1M-SM
J0660A	SC•PC-SC•PC-1M-SM
J1344A	LC•PC-LC•PC-1M-SM
J1139A	FC•PC-LC•PC-1M-SM
J1345A	SC•PC-LC•PC-1M-SM
J0893B	FC•PC-FC•PC-2M-GI (50/125)
J0894B	FC•PC-FC•PC-2M-GI (62.5/125)
J1346A	LC•PC-LC•PC-1M-GI (62.5/125)
J1347A	FC•PC-LC•PC-1M-GI (62.5/125)
J1348A	SC•PC-LC•PC-1M-GI (62.5/125)
J1359A	Coaxial Adapter (K-P, K-J, SMA)
J1360A	Measurement Kit <J1342A × 2, J1343A × 1>
J1449A	Measurement Kit (K connector) <J1439A × 2, J1342A × 2, J1343A × 1>
Z0282	Ferrule Cleaner
Z0283	Ferrule Cleaning Replacement Tape (6 pcs/set)
Z0284	Adapter Cleaner (Stick type, 200 pcs/set)
Z0897A	MP1800A Manual CD
Z0916A	Ferrule Side Face Cleaner
Z0917A	Shielded LAN Cable, 5 m (CAT5, Straight)
Z0918A	MX180000A Software CD
Z0922A	English USB Keyboard (104 key)
B0588A	Rack Mount Kit (MP1800A)
B0587A	Rack Mount Kit (MT1810A)
B0576A	Blank Panel
B0566A	MP1800A Hard Carrying Case (MP1800A)
B0591A	MT1810A Hard Carrying Case (MT1810A)
W2745AE	MP1800A Operation Manual
W2747AE	MP1800A Installation Guide
W2746AE	MT1810A Operation Manual
W2748AE	MT1810A Installation Guide
W2750AE	MU181000A/B Operation Manual
W2752AE	MU181020A/B Operation Manual
W2753AE	MU181040A/B Operation Manual
W3481AE	MU181500B Operation Manual
W2754AE	MU181600A/MU181601A Operation Manual
W2998AE	MU181620A Operation Manual
W2999AE	MU181640A Operation Manual
W2751AE	MU181800A/B Operation Manual
W3128AE	MU182020A/MU182021A Operation Manual
W3129AE	MU182040A/MU182041A Operation Manual
W2749AE	MX180000A Operation Manual
W2799AE	MX180000A Remote Control Operation Manual
W2884AE	MX180001A Operation Manual
W2885AE	MX180002A Operation Manual
W2886AE	MX180003A Operation Manual
W2887AE	MX180004A Operation Manual
W2926AE	MX180005A Operation Manual
W3480AE	MX181500A Operation Manual

∗1: The XFP module is sold separately.
Note that Anritsu supports only XFP modules purchased from Anritsu.
∗2: The SFP module is sold separately.
Note that Anritsu supports only SFP modules purchased from Anritsu.

Anritsu

Specifications are subject to change without notice.

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